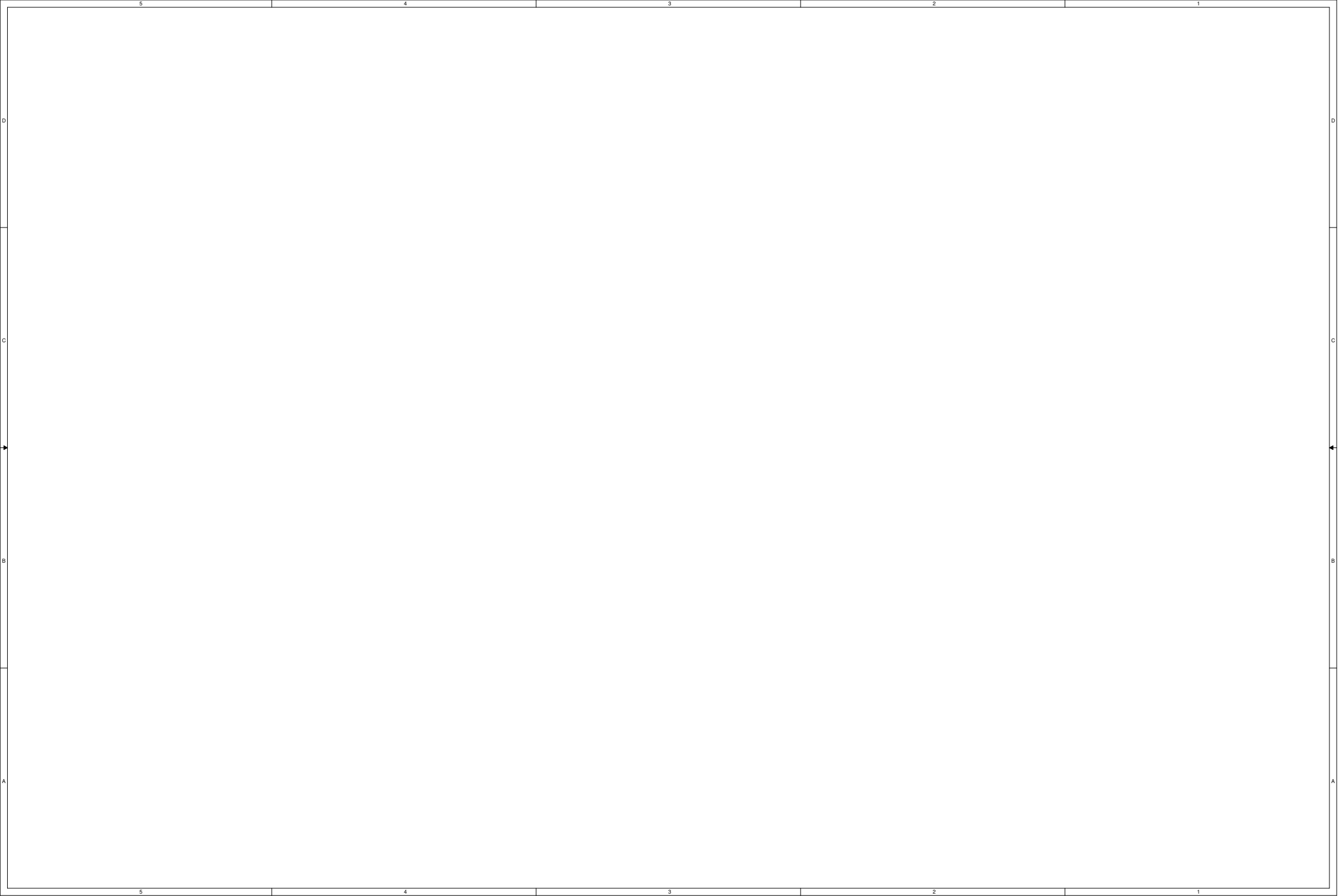
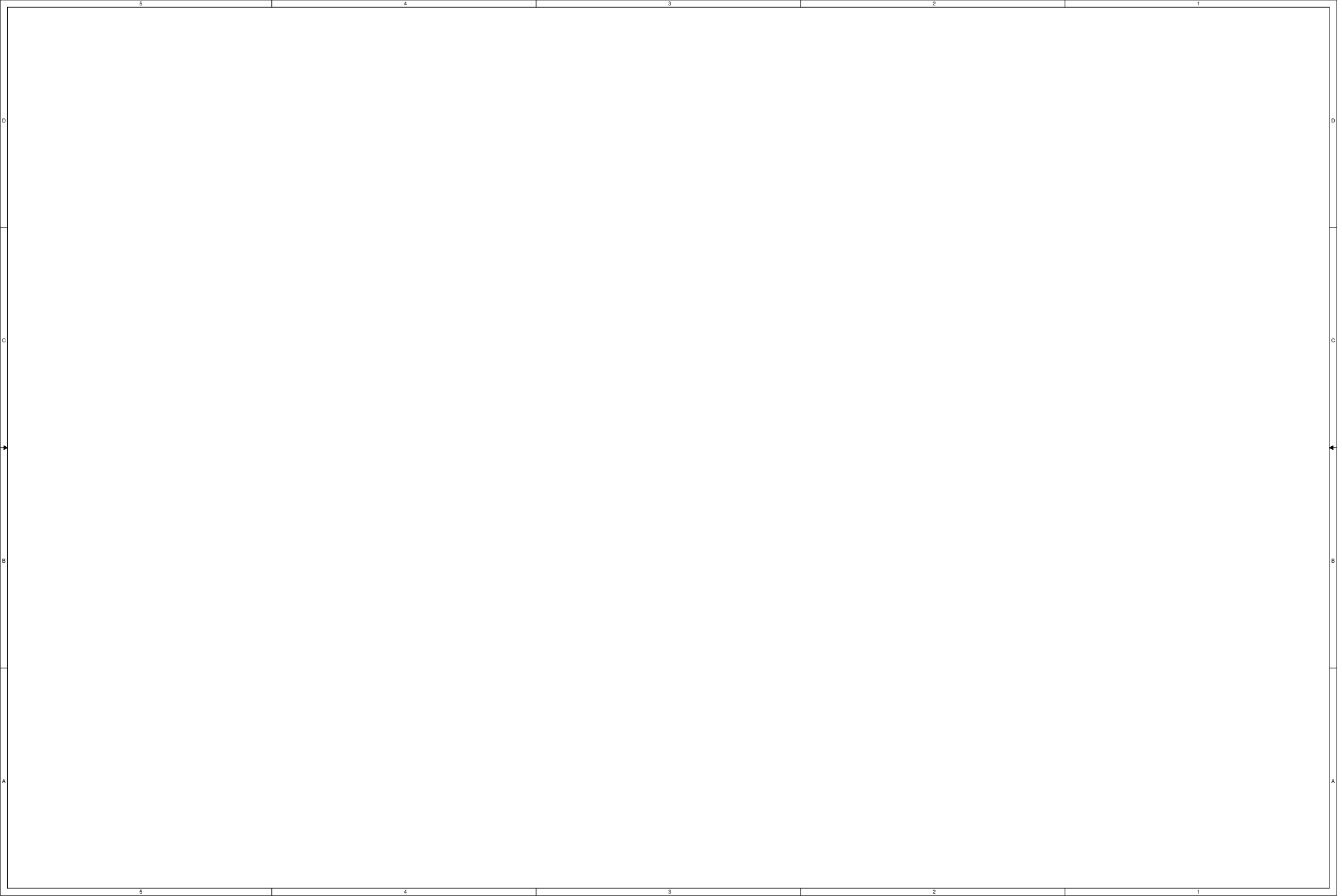
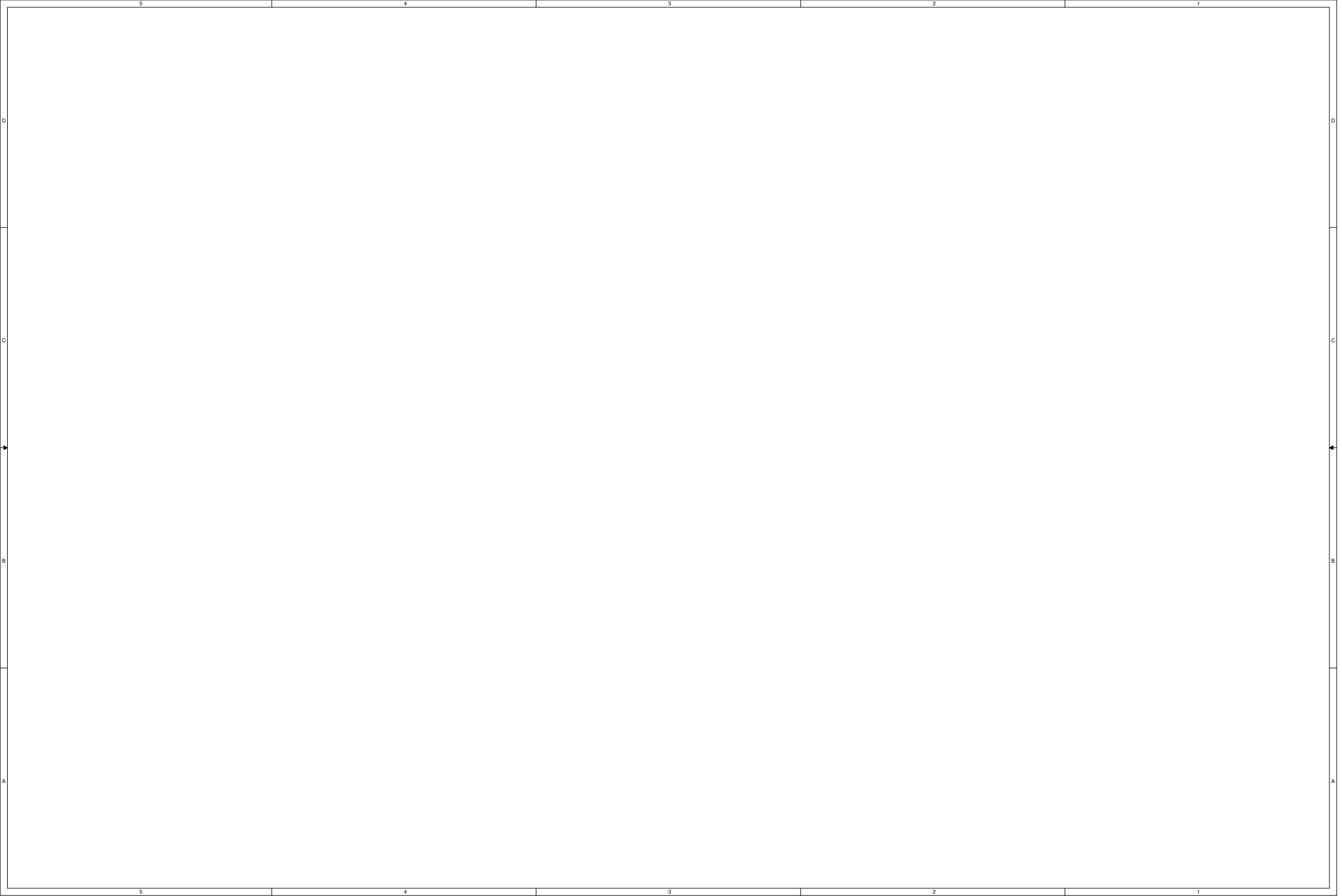
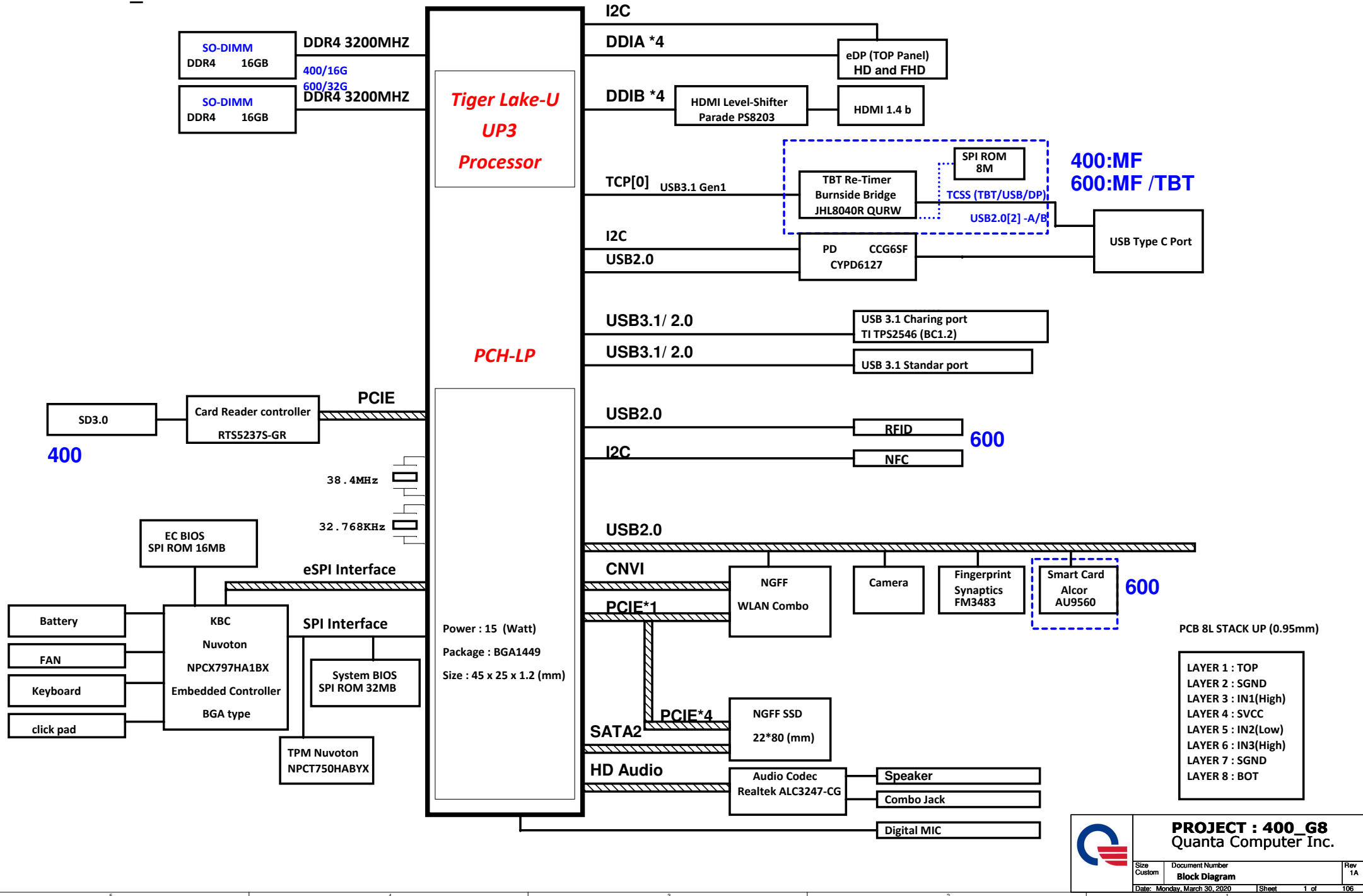




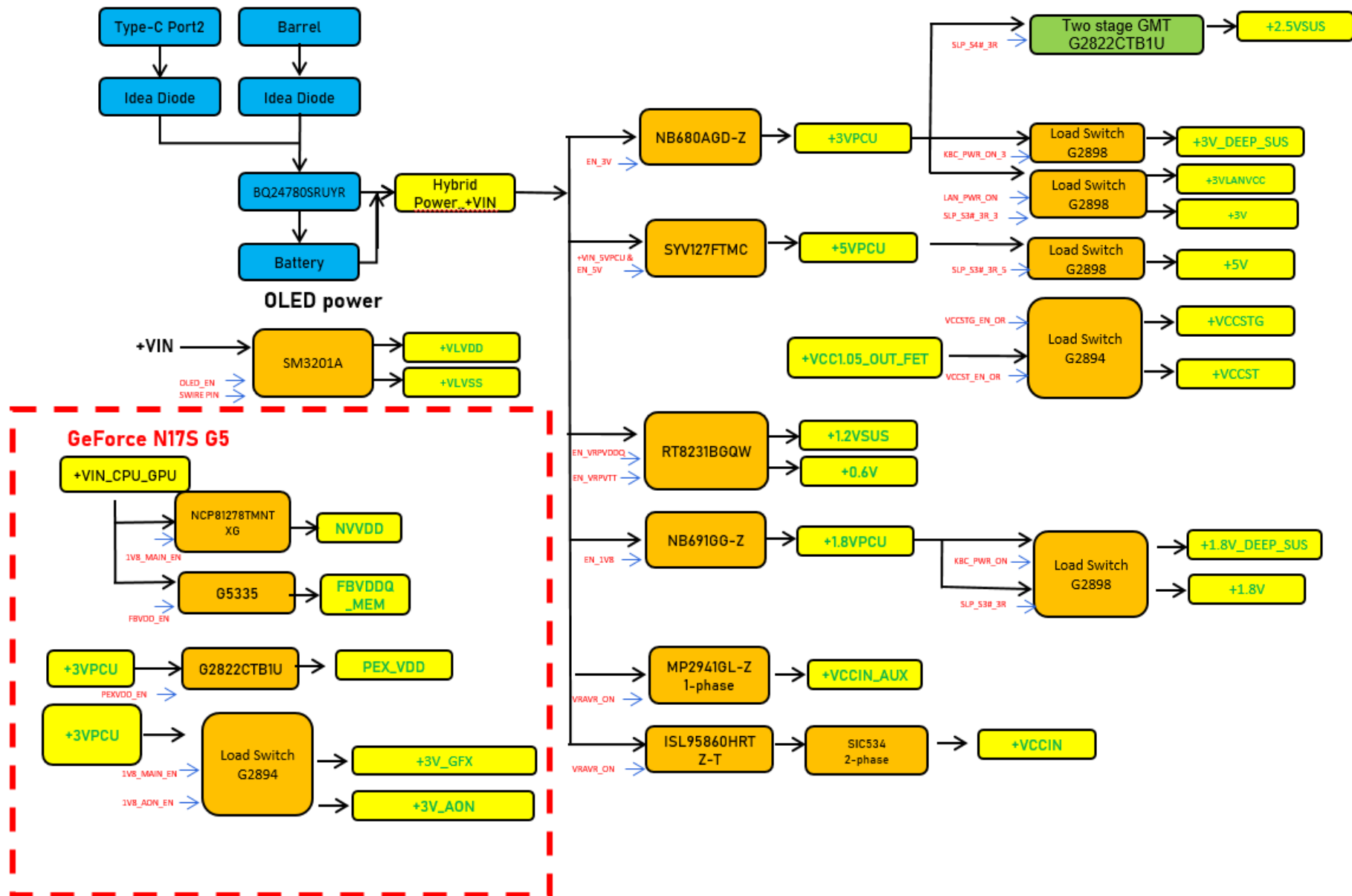


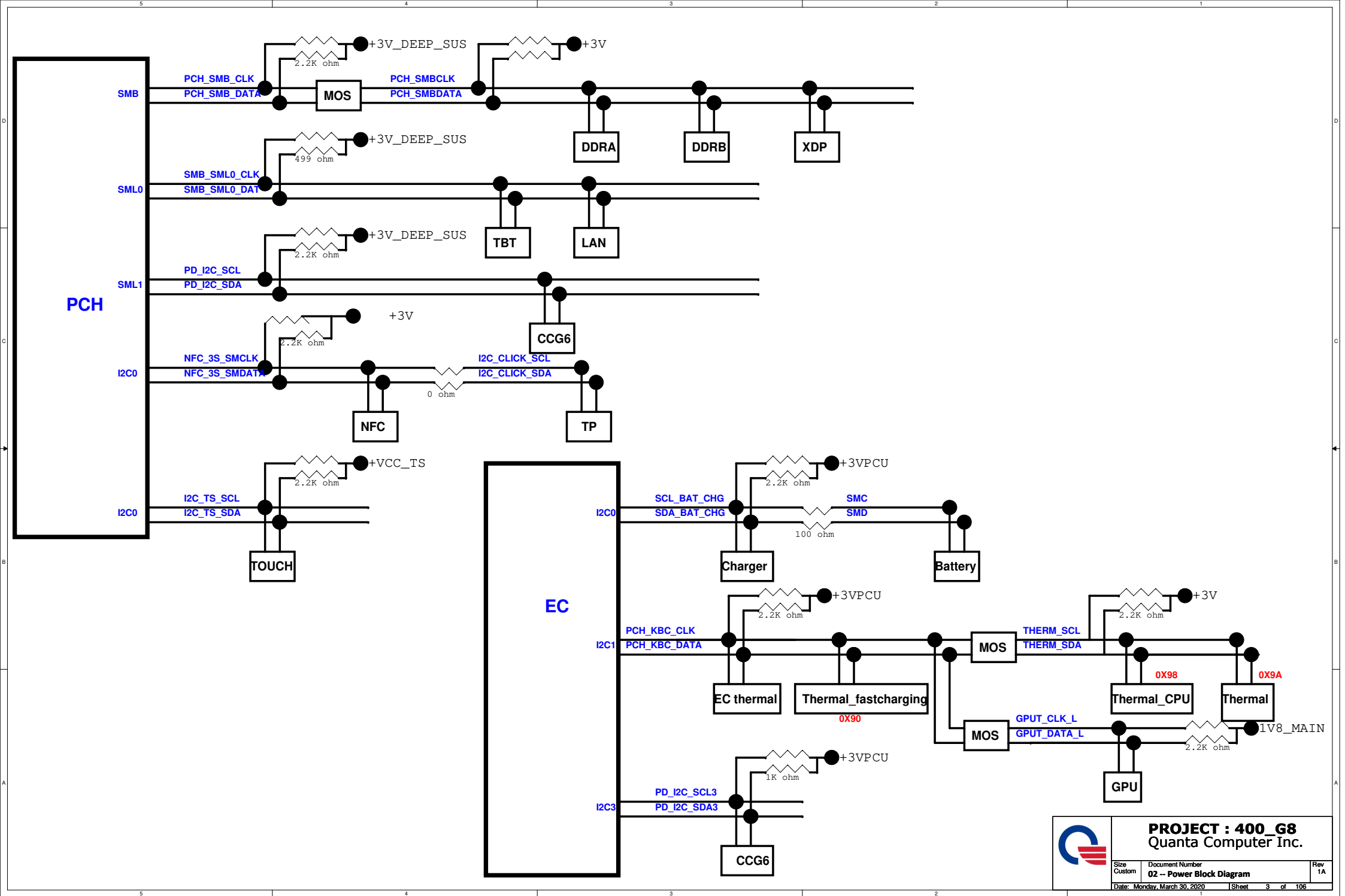


40013" G8_TGL



TGL-U POWER BLOCK DIAGRAM





eDP
2Lanes

HDMI

TBTA

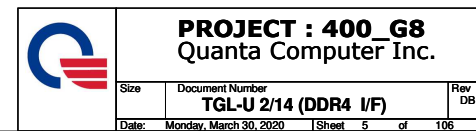
R401 100K 5% 2 CPU_EDP_HPD
need Check HPD Function

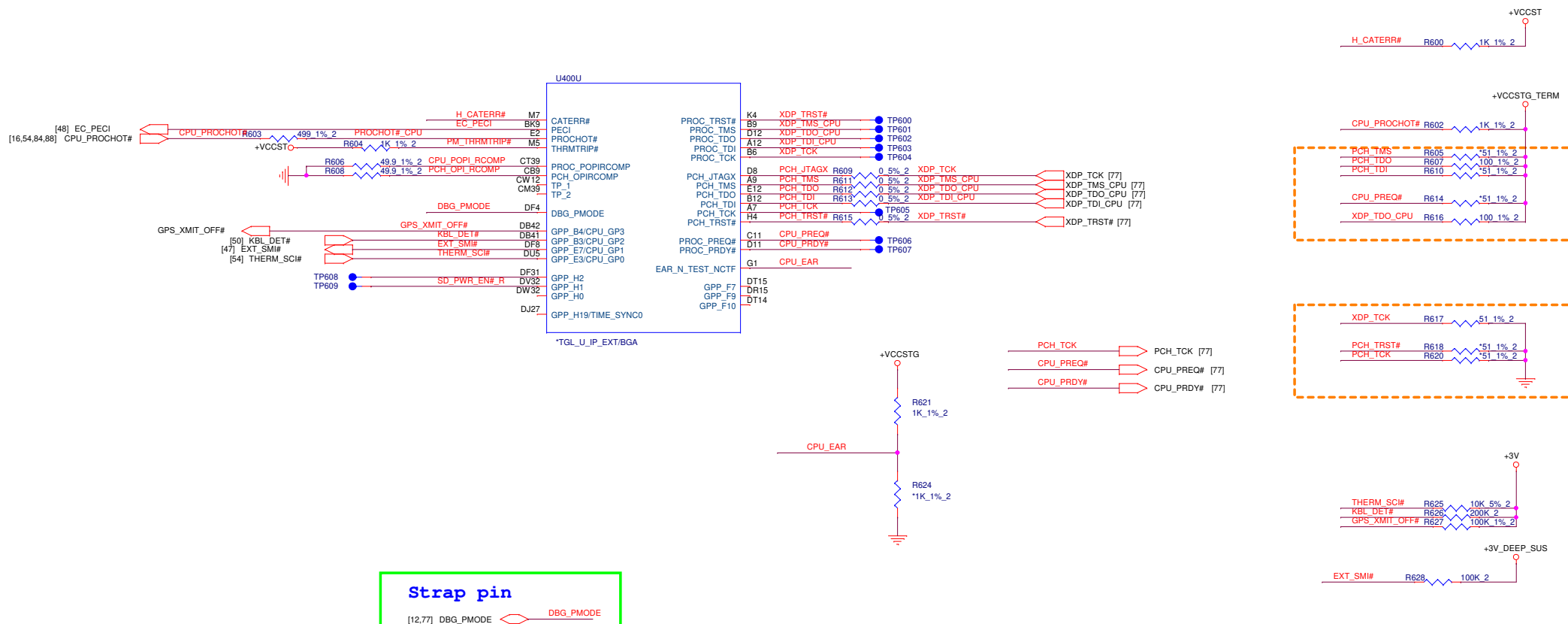
R404 100K 2% HDMI_HPD_CON
R405 100K 2% DDSP_1_HPD1
400 G8, 0102

+3V_DEEP_SUS
R406 *10K 5% 2 USB_OC1#
R407 *10K 5% 2 USB_OC2#

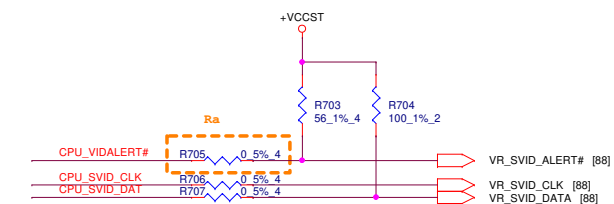
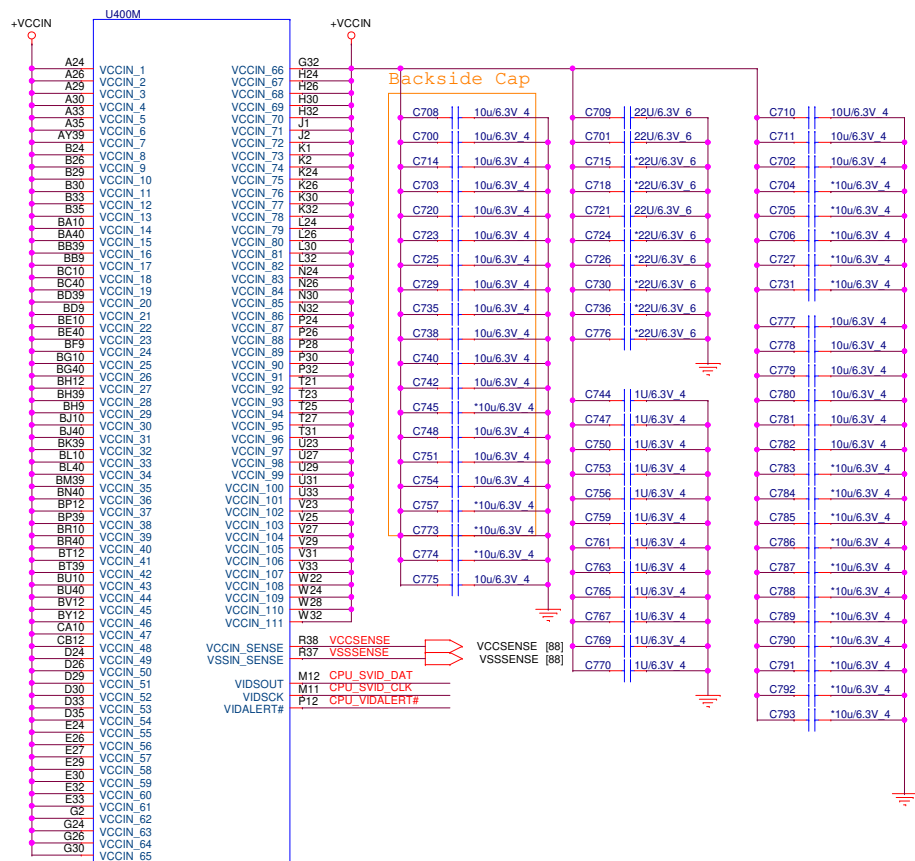
strap pin
[12] TBT_LXS2_RXD TBT_LXS2_RXD
[12] TBT_LXS3_RXD TBT_LXS3_RXD





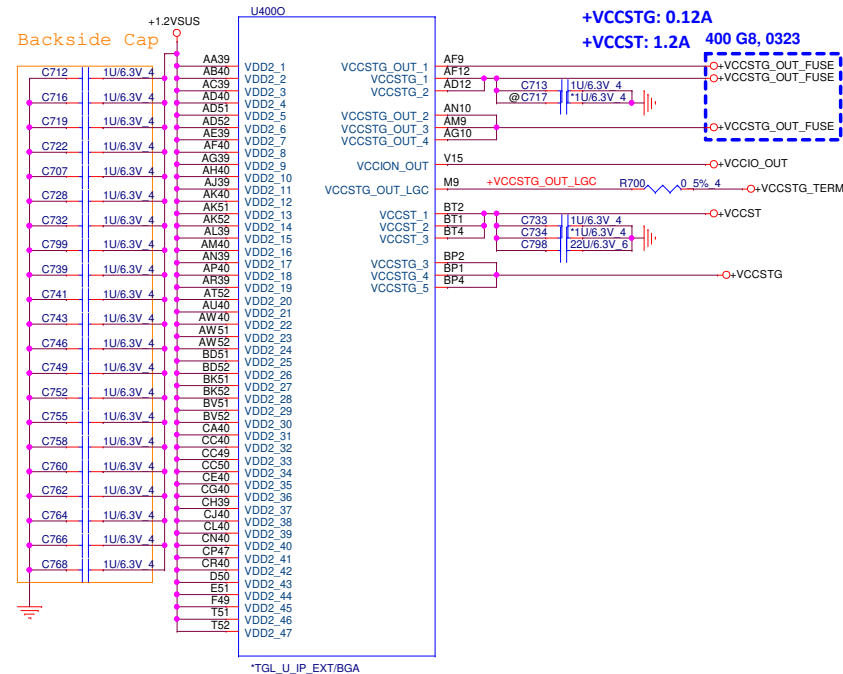


+VCCIN: 70A



ALERT# needs to Place between CLK and DAT
Ra Neen check value

400 G8, 0323

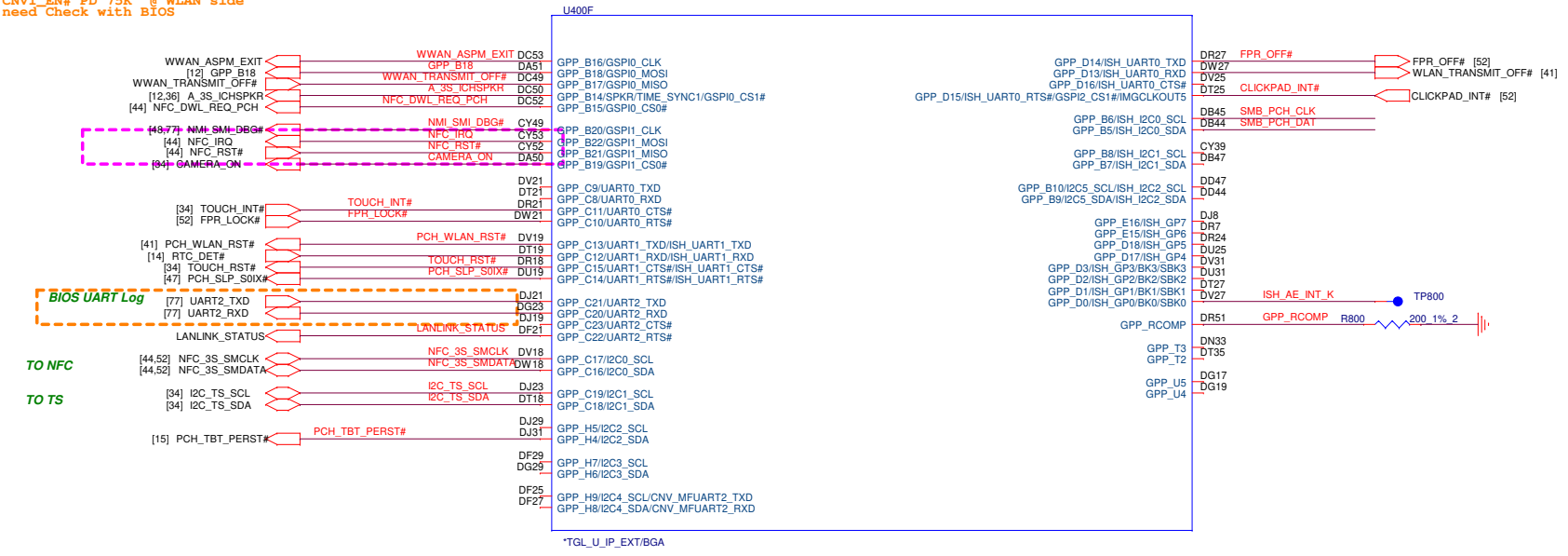


+VCCIN [88,89,97]

+VCCIO_OUT [10]
+VCCST [6,15,20,48,88,96]
+VCCSTG [6,96]

01/17 Add SOC_ENBK1 for S5 Turn off the Backlight

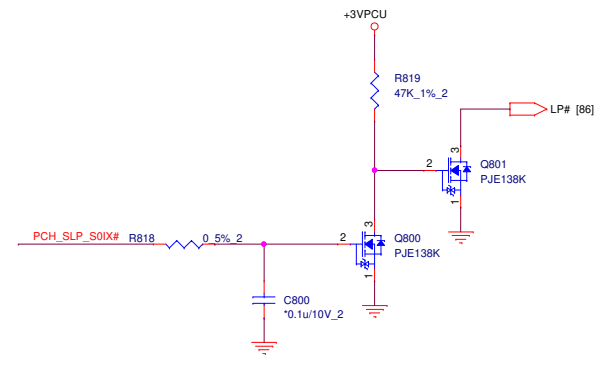
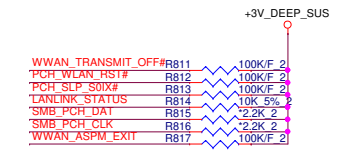
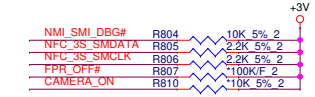
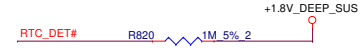
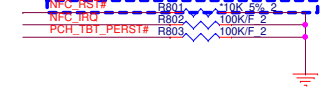
CNVI_EN# PD 75K @ WLAN side need Check with BIOS



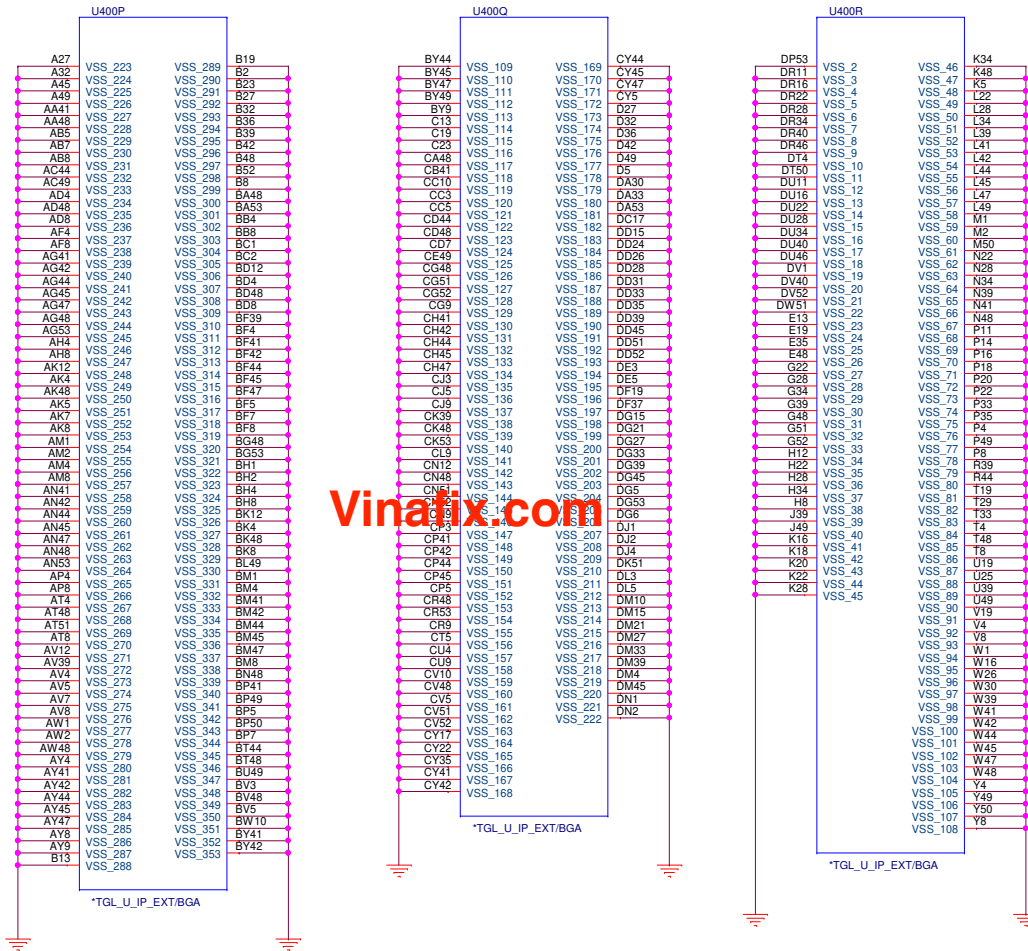
TO NFC

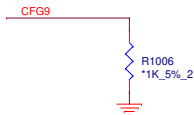
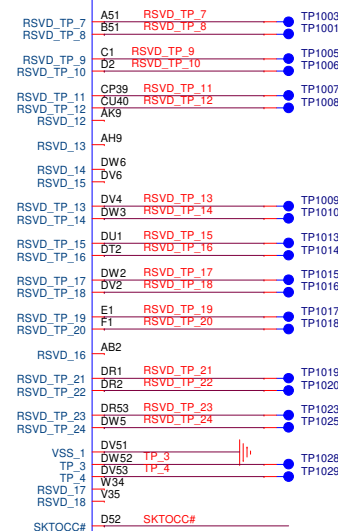
TO TS

400 G8, 0102

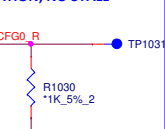
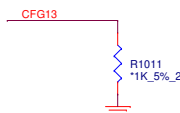
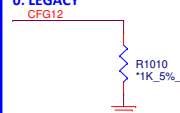
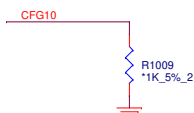


	PROJECT : 400_G8 Quanta Computer Inc.	
	Size Custom	Document Number TGL-U 5/14 (I2C/ISH)
	Date: Monday, March 30, 2020	Sheet 8 of 106



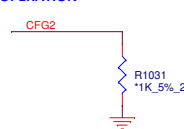


CFG13
1: (DEFAULT)SYNCHRONOUS (1 24 MHZ CYCLE PER BIT)
0: ASYNC - 4-24MHZ CYCLES PER BIT

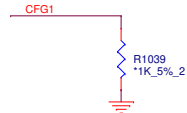
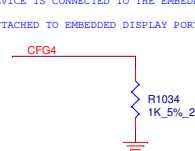


0: LANE REVERSAL


```
graph TD; CFG2[CFG2] --- R1031[R1031  
1K_5%_2]; R1031 --- GND[Ground]
```

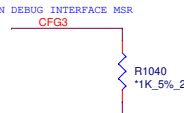


```
1: DISABLED
  AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
0: ENABLED
  NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
```

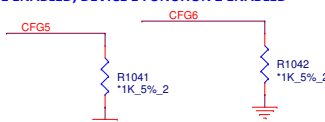


SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

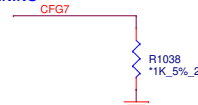
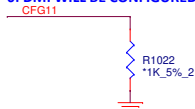
CFG3



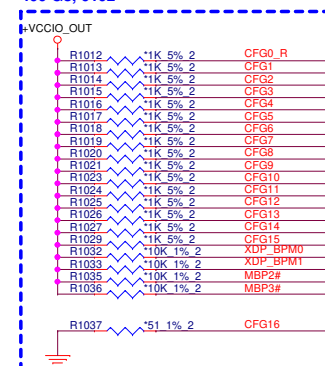
```
11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED
```



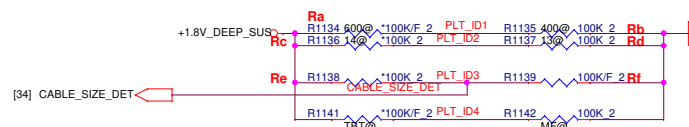
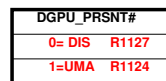
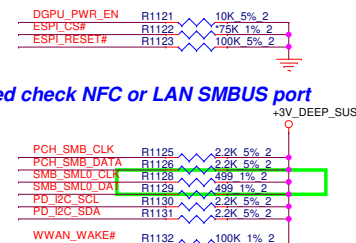
A circuit diagram showing a 1k resistor (R1022) connected between the CFG11 pin and ground. The resistor is labeled "R1022" and "1K_5%_2".



CFG8
1: DISABLE(DEFAULT): IN THIS CASE, NOA WILL BE
DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS
0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF
THE LOCKING OF THE UNIT



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Date: Tuesday, March 31, 2020		Sheet 10 of 106



PLT_ID2	PLT_ID3	
Rc	Re	H
Rd	Rf	L
0	0	13.3" UMA
1	1	14"
1	0	15.6"
0	1	17

PLT_ID4
0= MF
1=TBT+VPRO

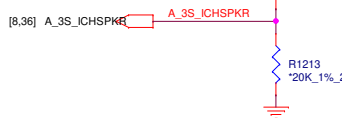
PLT_ID1
0= 400
1=600



TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

GPP_B14/SPKR

**NO REBOOT**

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

GPP_B18/GSPI0_MOSI

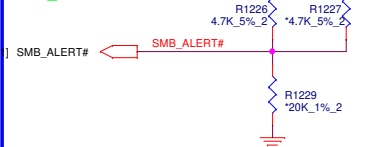


01/15 PD 10K at PAGE.8

TLS CONFIDENTIALITY

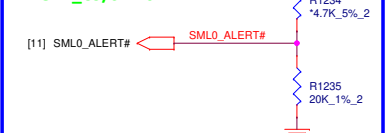
HIGH - TLS CONFIDENTIALITY ENABLE
LOW - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

GPP_C2/SMBALERT#

**ESPI OR EC LESS**

HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED
WEAK INTERNAL PD 20K

GPP_C5/SML0ALERT#

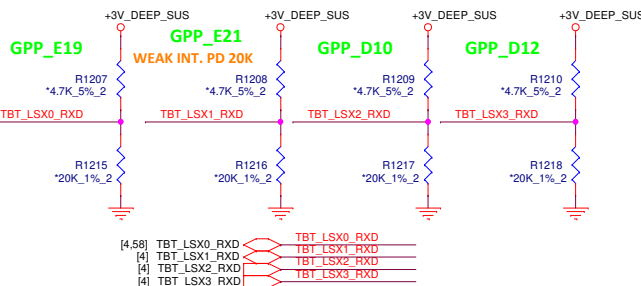
**(RSVD) ITP PMODE**

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

ITP_PMODE

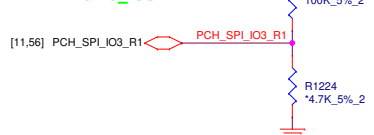
**TBT LSX PINS VCCIO CONFIGURATION**

High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD

**(RSVD) A0 PERSONALITY STRAP**

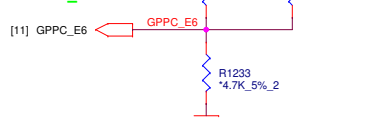
High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO3

**(RSVD) JTAG ODT DISABLE**

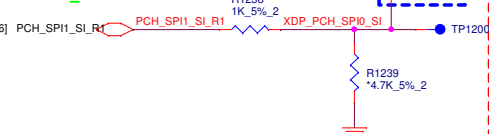
High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

GPP_E6

**(RSVD) BOOT HALT**

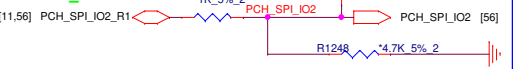
High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_MOSI

**(RSVD) CONSENT STRAP**

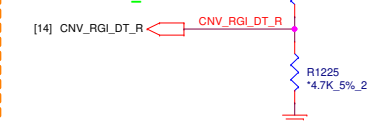
High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO2

**M.2 CNVi Mode Select**

High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required

GPP_F2

**(RSVD) XTAL INPUT MODE**

High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

RING OSCILLATOR BYPASS

High: BYPASS MODE ENABLED
Low: RING OSCILLATOR
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_H3

**Flash Descriptor Security Override**

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

GPP_R2

**CPUNSSC CLOCK FREQ**

High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

GPP_B23/SML1ALERT#

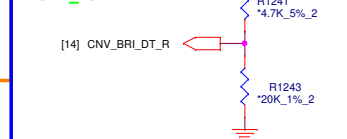


HVM ONLY

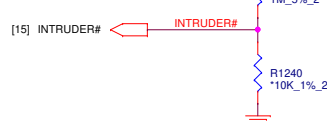
XTAL FREQUENCY SEL

High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

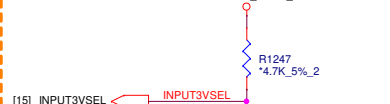
GPP_F0



GPP_E11

INTRUDER#**3V SELECT STRAP**

0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)



HVM ONLY



PROJECT : 400_G8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TGL-U 9/14 (HW STRAP)	1A
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	BOARD ID1	BOARD ID2	BOARD ID3	BOARD ID4
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
	0	0	1	1
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
	0	1	1	1
SI3	1	0	0	0
PV	1	0	0	1
PVR	1	0	1	0
	1	0	1	1
MV	1	1	0	0

PCI-E Port	Function	CLK RQ Port	Function
Port1	Type-A	Port0	SSD
Port2	Type-A	Port1	WWAN
Port3	WLAN	Port2	LAN
Port4	Type-A	Port3	GPU
Port5	NC	Port4	WLAN
Port6	SD	Port5	SD
Port7	WLAN		
Port8	NC		
Port9	PCI-E-SSD		
Port10	PCI-E-SSD		
Port11	PCI-E-SSD		
Port12	PCI-E-SSD		

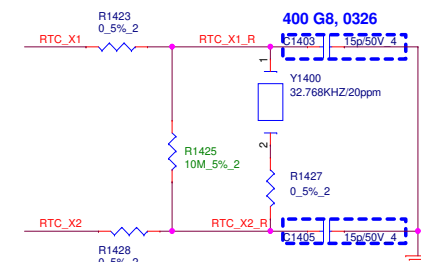
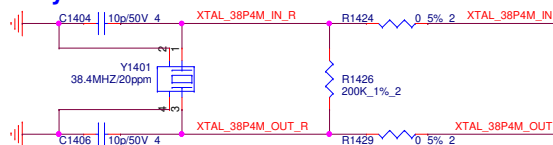
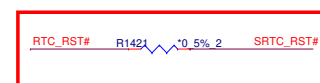
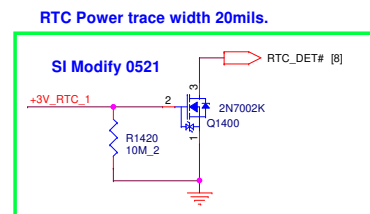
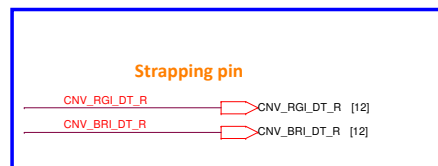


USB2.0	Function
PORT-1	USB A
PORT-2	Camera
PORT-3	Smart Card
PORT-4	NC
PORT-5	Type C
PORT-6	USB A
PORT-7	Finger Print
PORT-8	NC
PORT-9	RFID
PORT-10	BT

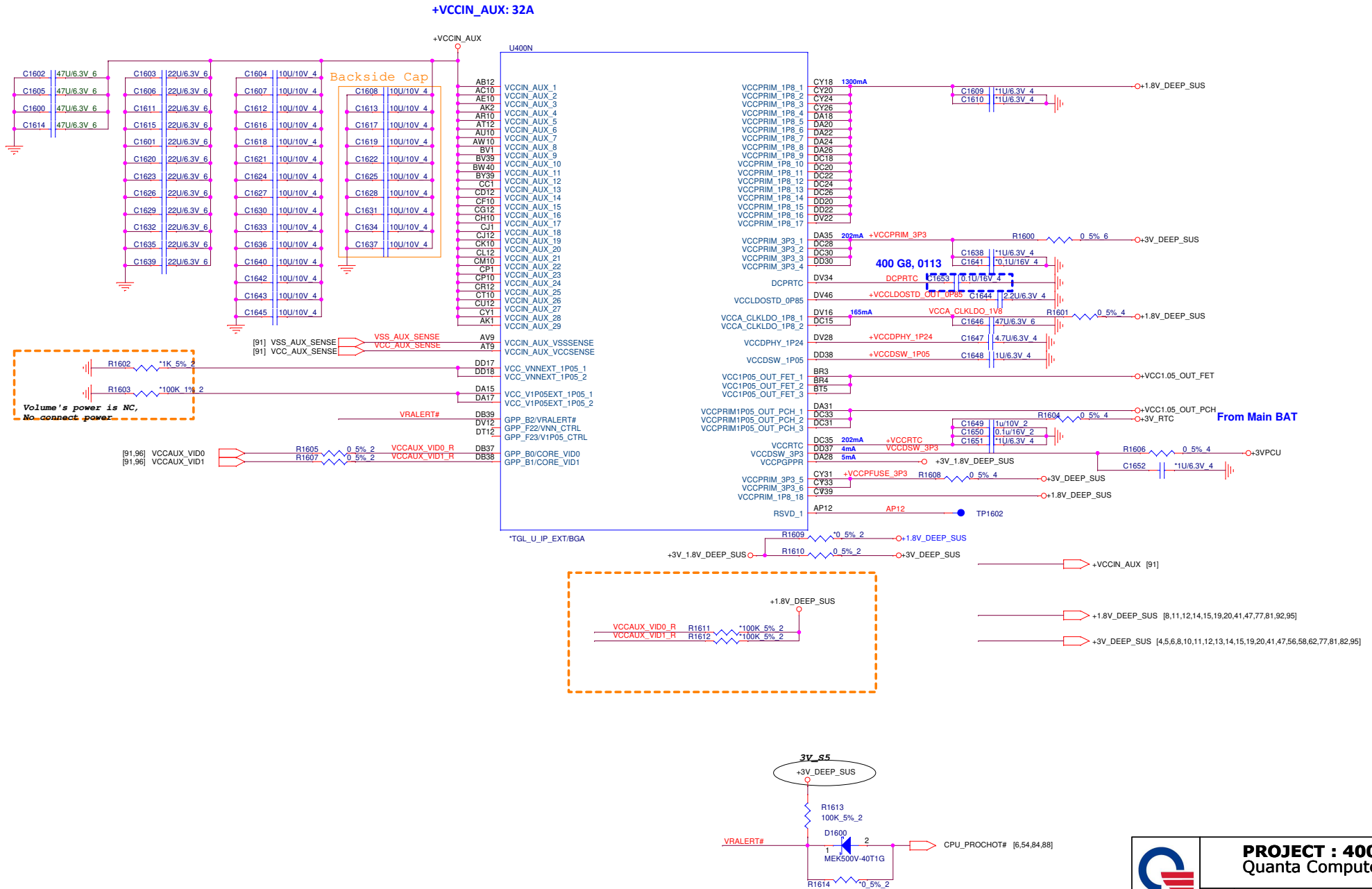
(Gen4)	Function
PORT-1	NC
PORT-2	NC
PORT-3	NC
PORT-4	NC



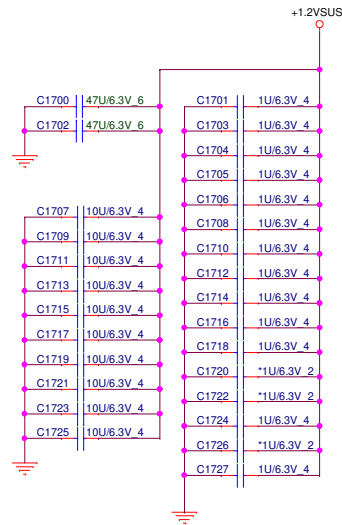
Size Custom	Document Number TGL-U 10/14(USB/PCIE/SAT)	Rev 1.
Date: Tuesday, March 31, 2020		Sheet 13 of 106

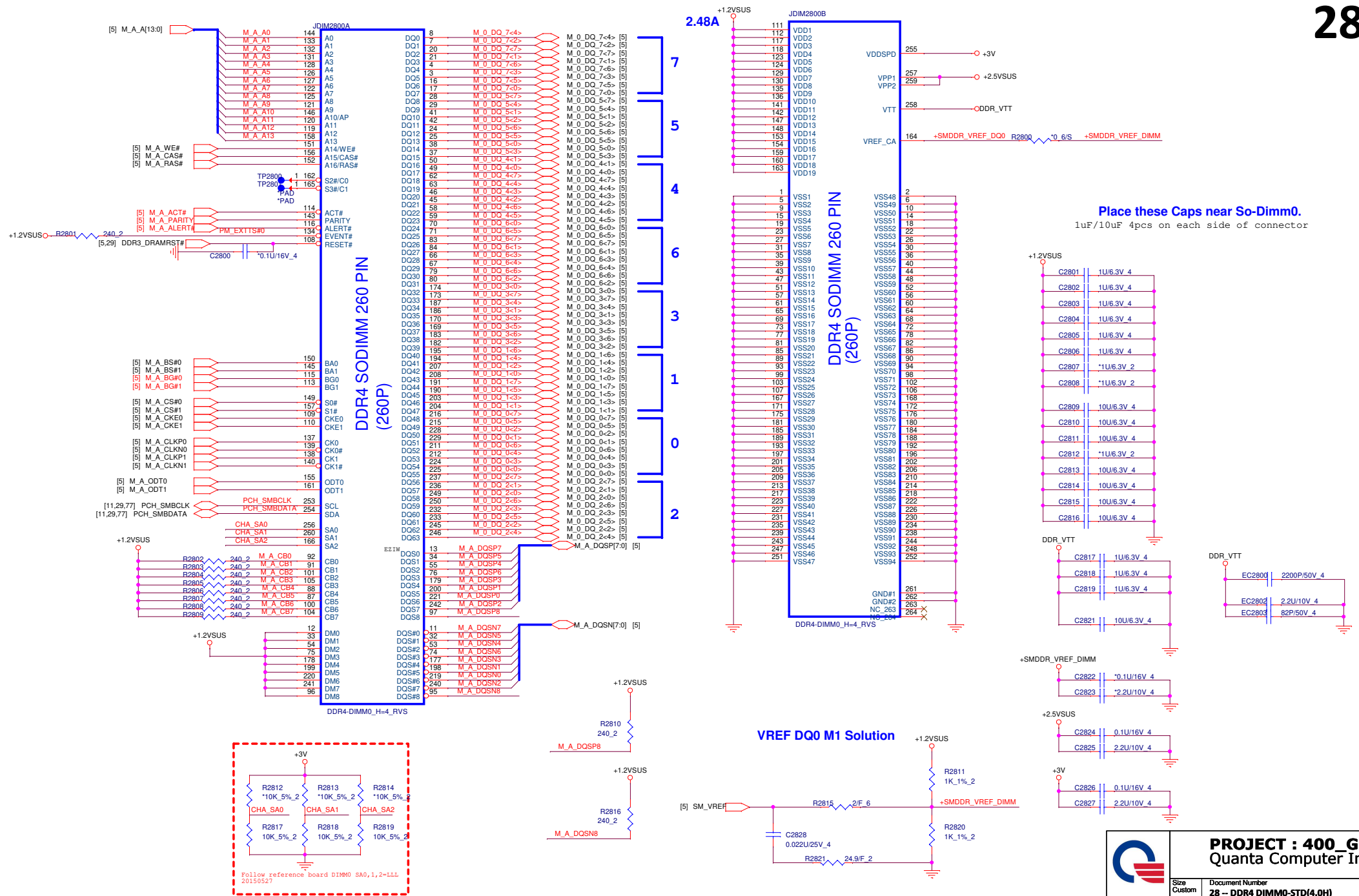


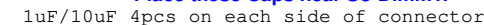




For page rule move the caps from page7 to page 17

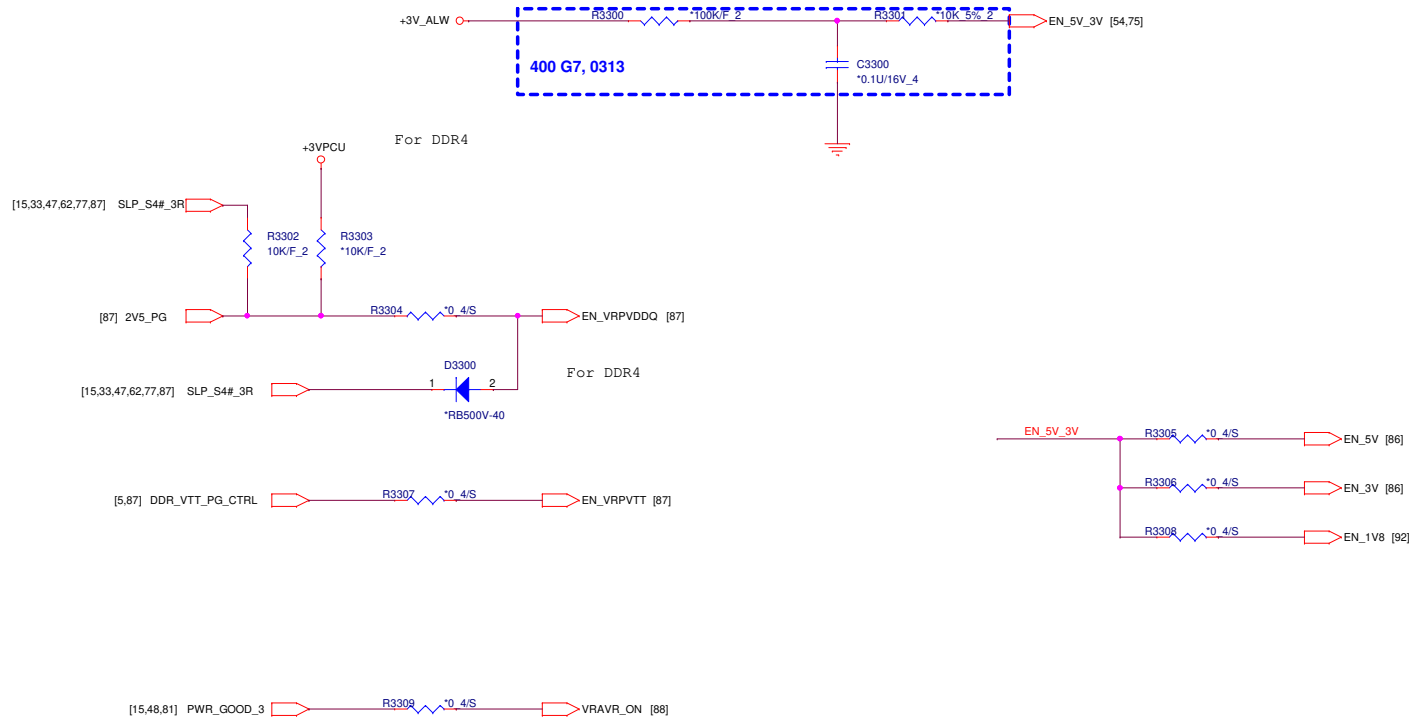




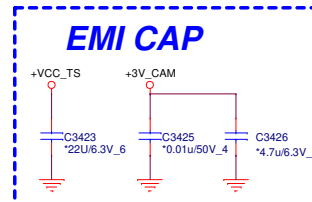
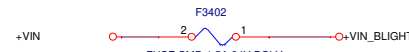
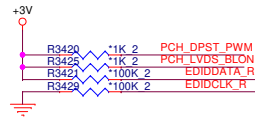
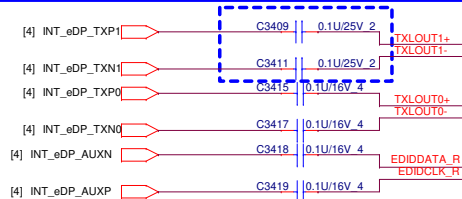
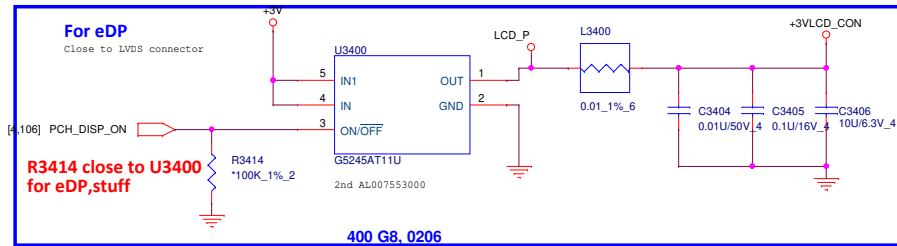
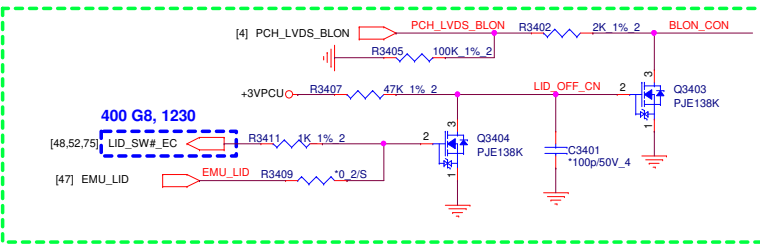


400 series 1001

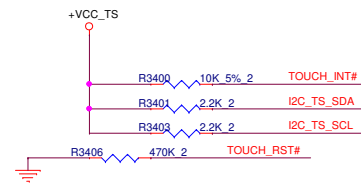
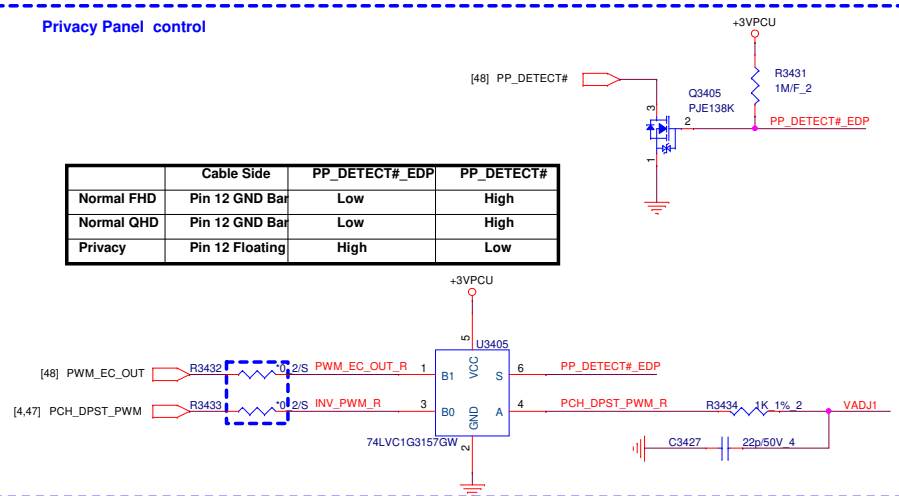
POWER TO EE NET NAME CONNECTION



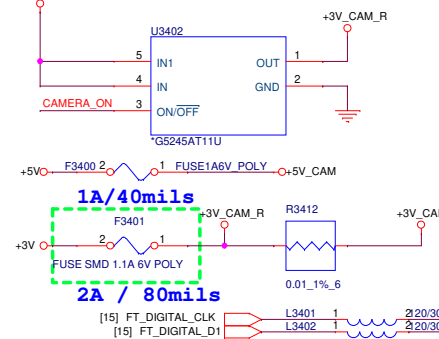
LID Switch



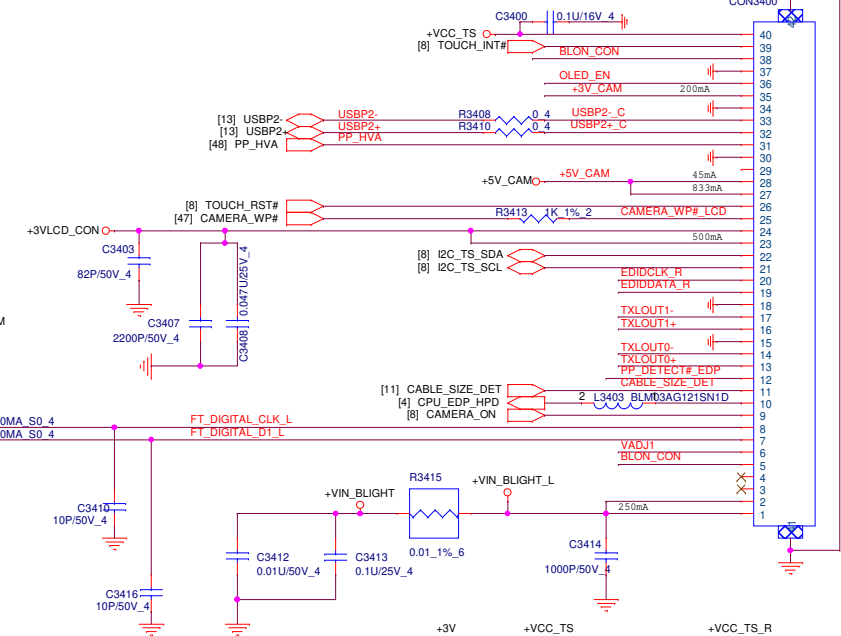
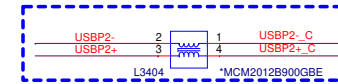
	Cable Side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 12 GND Bar	Low	High
Normal QHD	Pin 12 GND Bar	Low	High
Privacy	Pin 12 Floating	High	Low



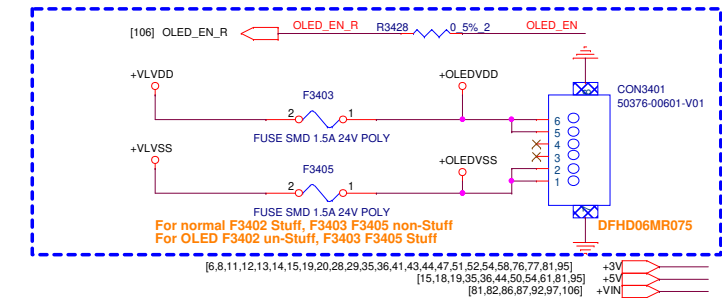
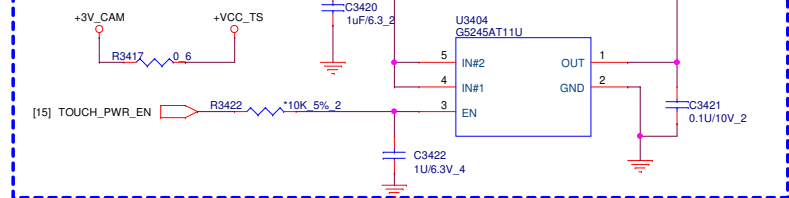
Cam Power



EMI CAP



```
for TS power
```



PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 34 -- LCD CONN/LID/CAM/D-MIC	Rev 3A
Date: Tuesday, March 31, 2020		Sheet 34 of 106

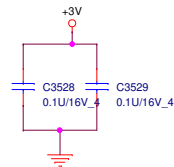
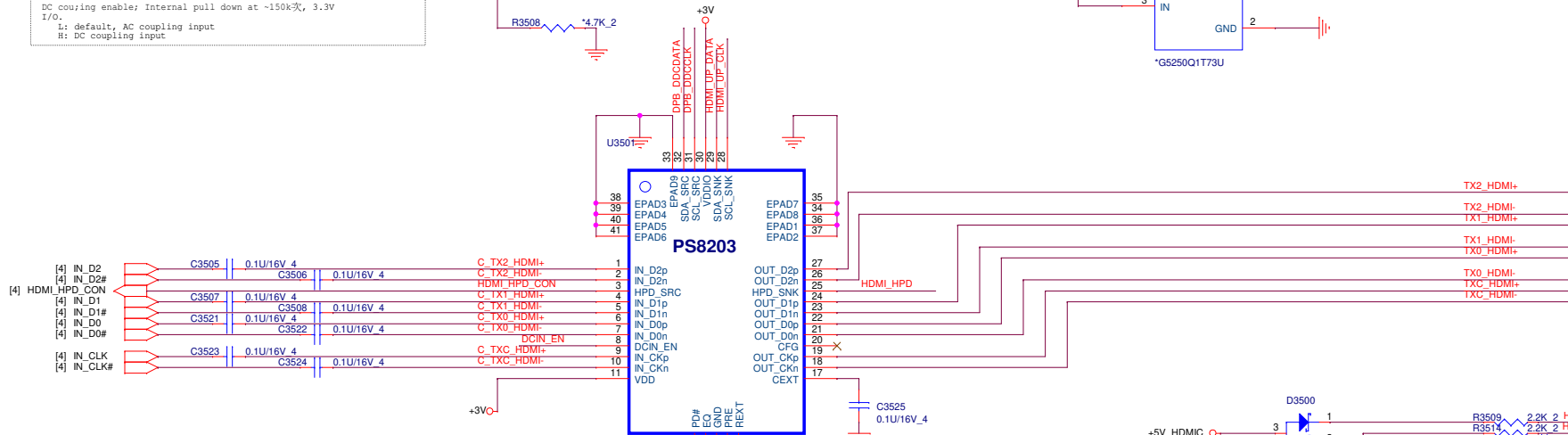
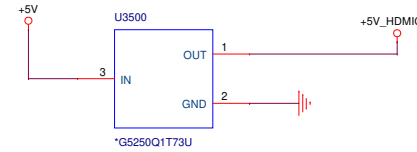
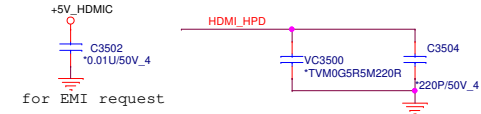
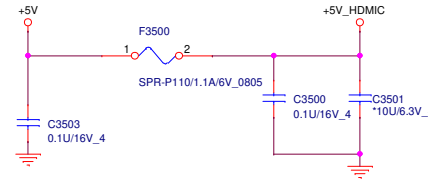
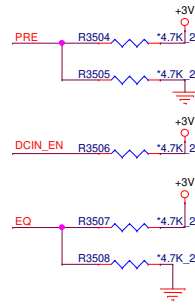
EMI Solution

TX2_HDMI+	R3500	150 5% 2	TX2_HDMI-
TX1_HDMI+	R3501	150 5% 2	TX1_HDMI-
TX0_HDMI+	R3502	150 5% 2	TX0_HDMI-
TXC_HDMI+	R3503	150 5% 2	TXC_HDMI-

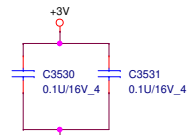
Output pre-emphasis setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

DC coupling enable; Internal pull down at ~150k Ω , 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

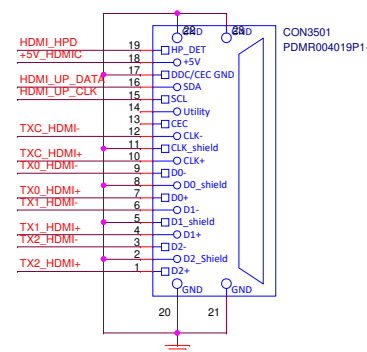
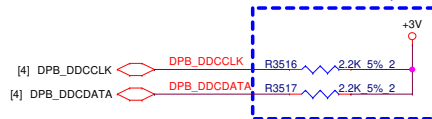


VDD for PS8203:
Power supply at 3.3V



VDDIO:
Supply voltage for DDC passive gate and used to set HPD_SRC output level
Its range can be 1.2V~3.6V

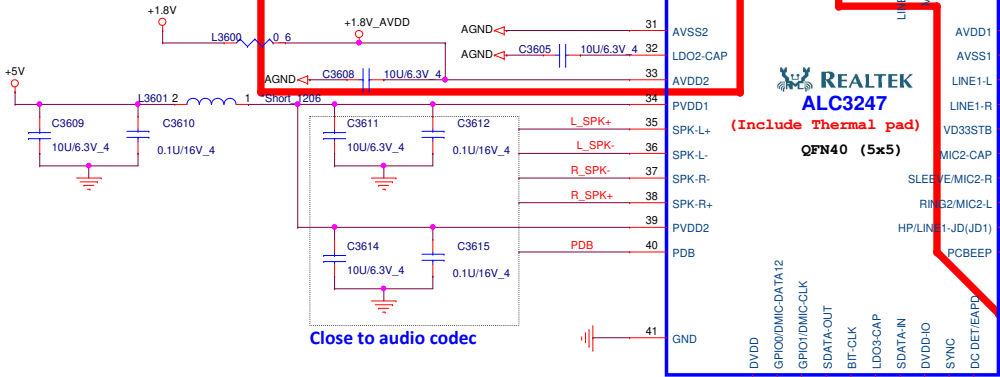
HDMI SMBus Isolation



Audio Codec

36

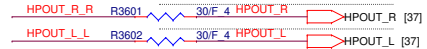
ANALOG
DIGITAL



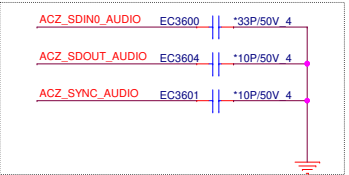
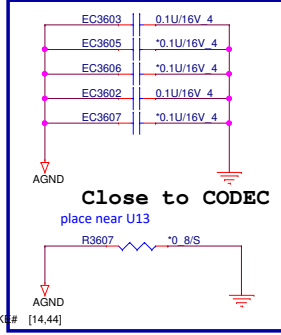
Close to audio codec

Close to PIN1

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible

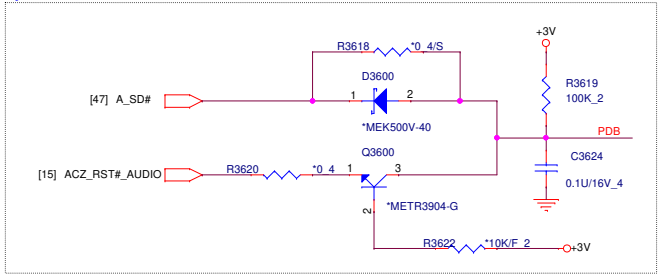


AGND SHIELD
AGND SHIELD TO Headphone jack
AGND SHIELD



ANALOG
DIGITAL

Speaker Power Down Control Circuit

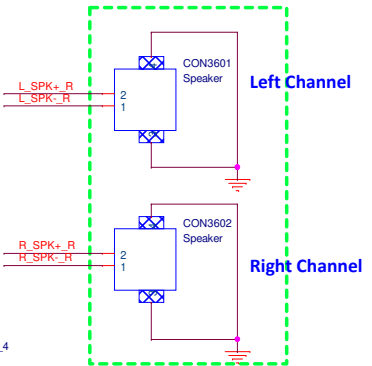
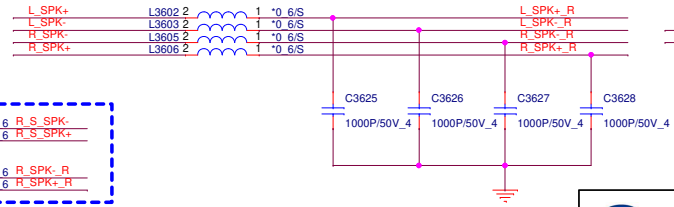
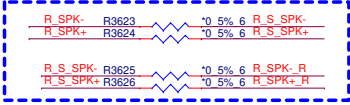


Internal Speaker

Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

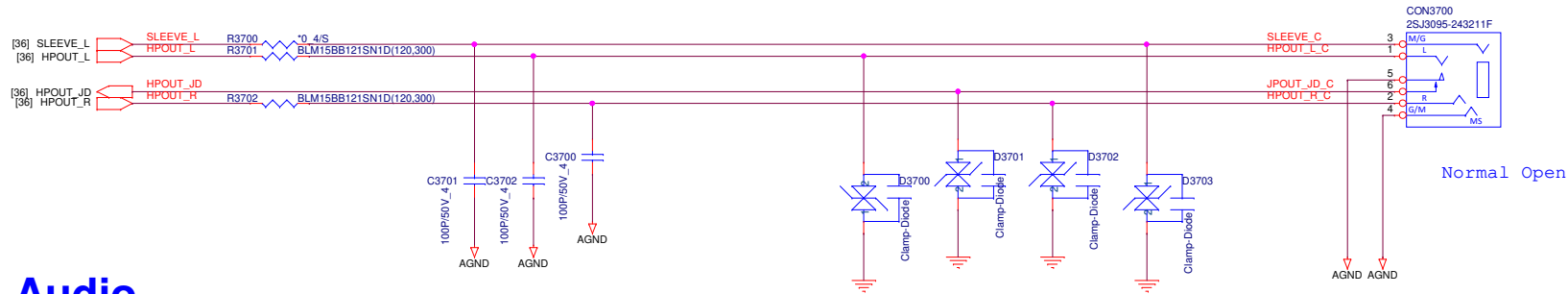
Close to Speaker

For SPK R Channel



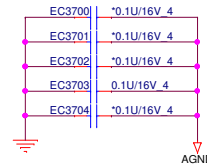
[11,18,81,95] +1.8V
[6,8,11,12,13,14,15,19,20,28,29,34,35,41,43,44,47,51,52,54,58,76,77,81,95] +3V
[15,18,19,34,35,44,50,54,61,81,95] +5V

 PROJECT : 400_G8 Quanta Computer Inc.		
Size Custom	Document Number 36 -- Audio Codec CX7501	Rev 3A
Date: Tuesday, March 31, 2020	Sheet 36 of 106	



Audio

All Clamp-Diode need close to ADO Jack.





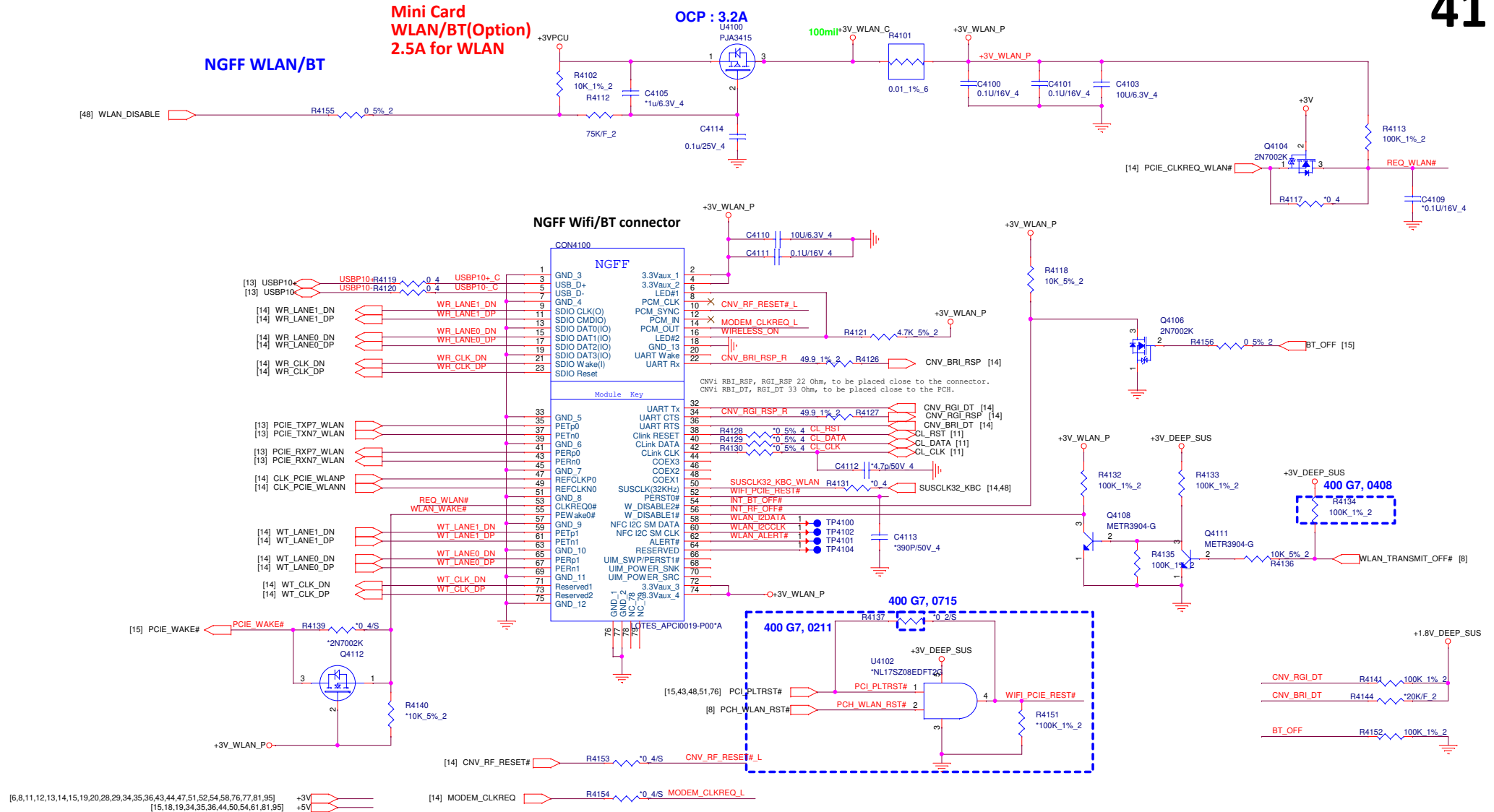
PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 40 – LAN RTL8111HSH-CG/RJ45	Rev 3A
Date: Monday, March 30, 2020		Sheet 40 of 106

**Mini Card
WLAN/BT(Optional)
2.5A for WLAN**

OCP : 3.2A

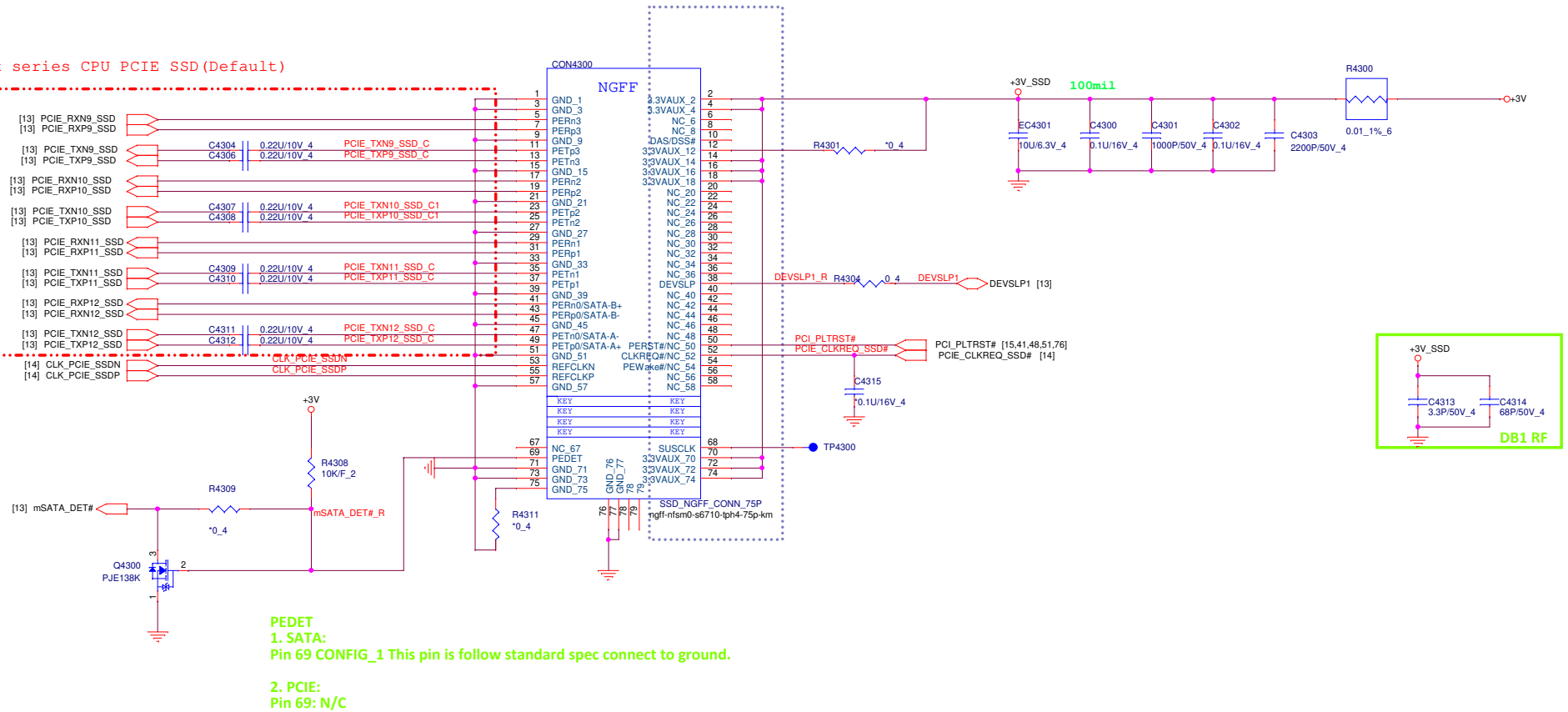
NGFF WLAN/BT



PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 41 -- NGFF WLAN/BT	Rev 3A
Date: Monday, March 30, 2020	Sheet 41 of	106

For Ix series CPU PCIE SSD(Default)



[6,8,11,12,13,14,15,19,20,28,29,34,35,36,41,44,47,51,52,54,58,76,77,81,95]

+3V

Address: 0x2XX(7 bit)

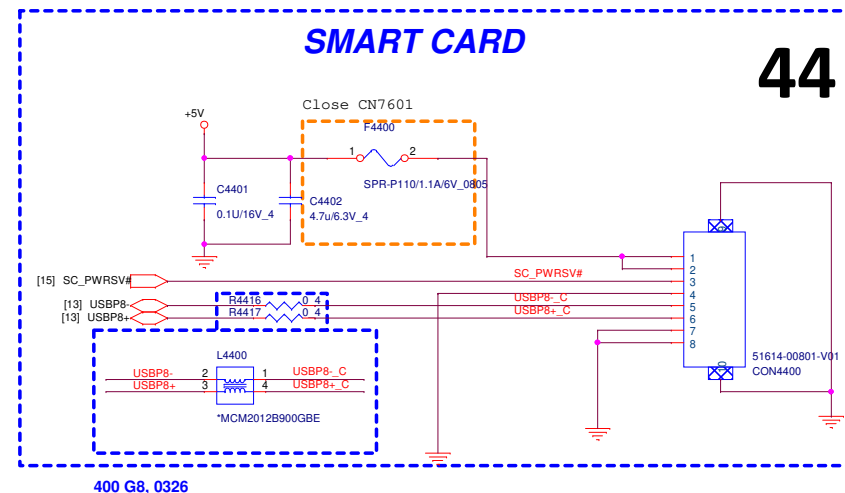
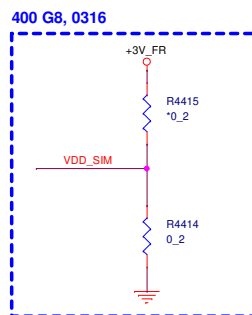
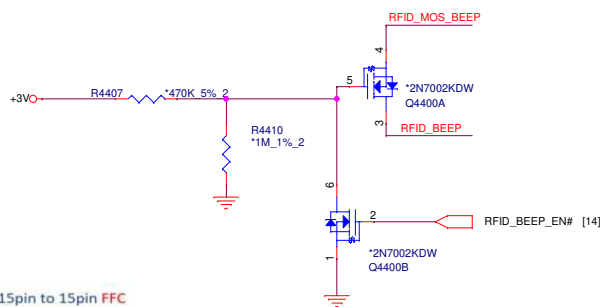


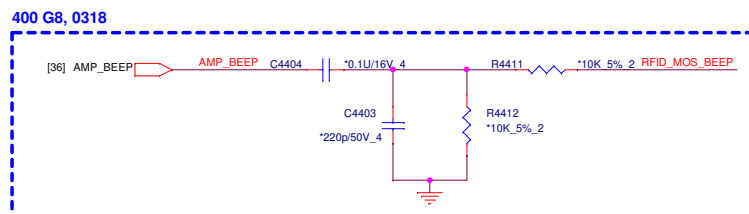
Figure 1-10 shows the NFC Tag I2C SCL and SDA Connections. The diagram illustrates the pin connections for the NFC tag (NFC_TAG_I2C_SDA, NFC_TAG_I2C_SCL) to the system. The tag is connected to the system via a 4-pin connector. The connections are as follows:

- Pin 1: +3V_FR
- Pin 2: NFC_RST#
- Pin 3: NFC_TAG_INT#
- Pin 4: Ground
- Pin 5: TILE_TAG_I2C_SCL
- Pin 6: TILE_TAG_I2C_SDA
- Pin 7: Ground
- Pin 8: Ground

The tag is labeled *51614-00801-V01 CON7704.



Vinafix



Pin	Symbol	Description
1	VCC	External Power Supply (3.3V)
2	VEN#	Mux Enable, Low Active
3	FD	Field Detection
4	GND	GND/HW Detect
5	GND	GND
6	SCL	I2C Clock
7	SDA	I2C Data
8	VOUT	Energy Harvesting

Pinout Tables

MODULE CONNECTOR (RFID)

Pin number	Name
1	USB V+
2	USB D-
3	USB D+
4	GN
5	Audio Feedback BEEP – Output
6	Low Power Mode – Input
7	Card Read – Output
8	Module detect# – Output (TBD)****
9	GN
10	GN

****RFID module pin8 is a multiple-function pin but is NOT used in HP platforms. For FPC design, do NOT connect this pin to host connector pin15 (just left open).

HOST CONNECTOR

Pin number	Pin Name	Notes
1	NFC_NCD_VDD0	Connects to Vcc for NFC
2	GND	For NFC and RFID
3	VDDnB	For RFID
4	NFC_NCD_VDD0 (also for RFID_VDDnB)	Connects to Vcc for both NFC and RFID
5	NFC_MADQ_VDD0 and I/O (chip select)	For NFC and RFID
6	NFC_NCD_VSS	Connects to GND for NFC
7	NFC_NCD_VSS	For NFC
8	NFC_NCD_SCL	For NFC
9	GND	For NFC and RFID
10	NFC_MADQ_I2T (Input) NFC_NCD_I2T (Input) Ruster (RFID) I2T (Output)	For NFC or RFID**
11	NFC_NCD_VDD0	For NFC
12	GND	For RFID
13	NFC_NCD_VDD0	Connects to Vcc for NFC
14	NFC_NCD_VSS	Connects to GND for NFC and RFID
15	Variable Dependency Input	

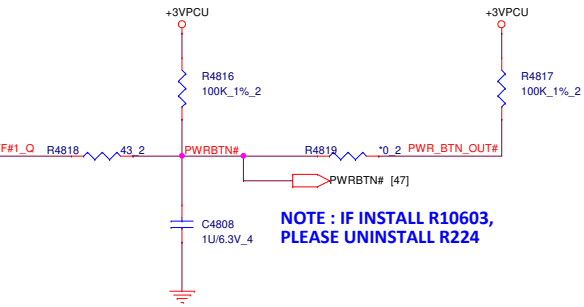
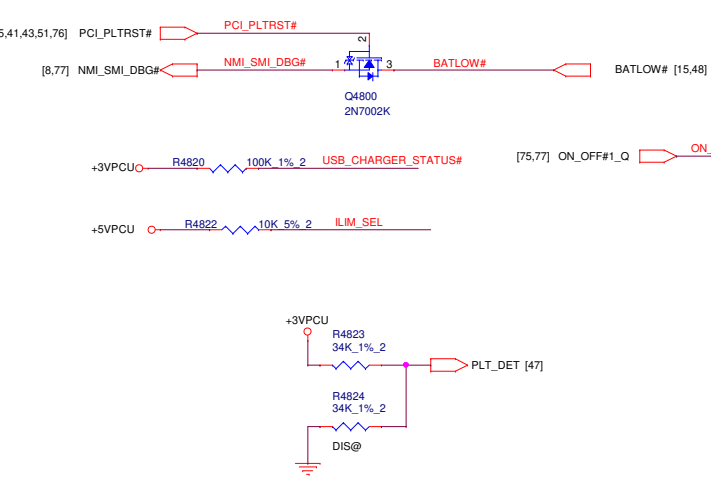
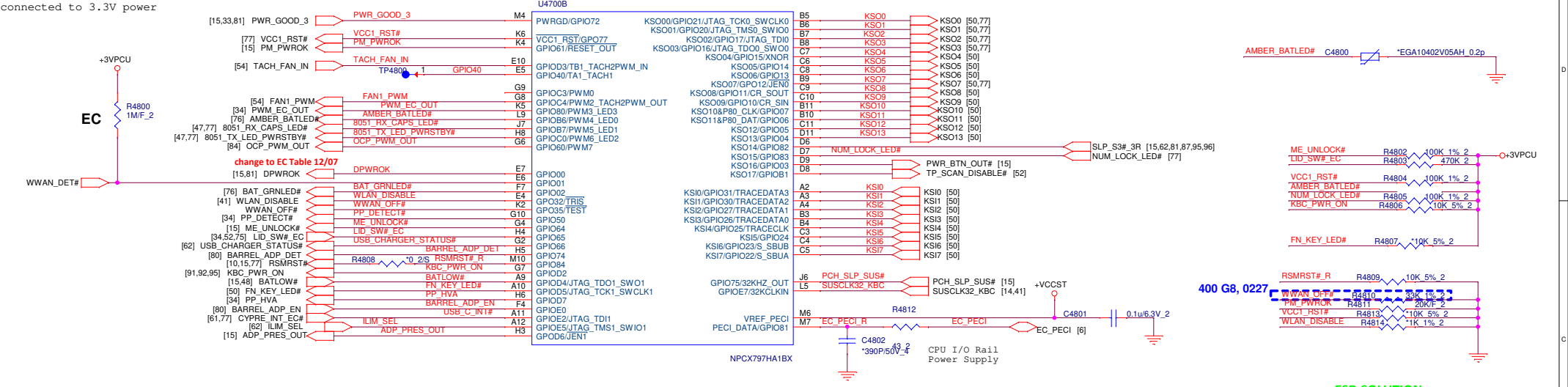
***NFC_DWL_RFO will be repurposed to use as beep signal to PCH with RFID installed.



PROJECT : 400_G8
Quanta Computer Inc.

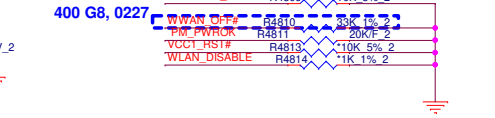
Size Custom	Document Number 44 -- NFC/RFID/SMART CARD	Rev 3A
Date: Tuesday, March 31, 2020	Sheet 44 of	106

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

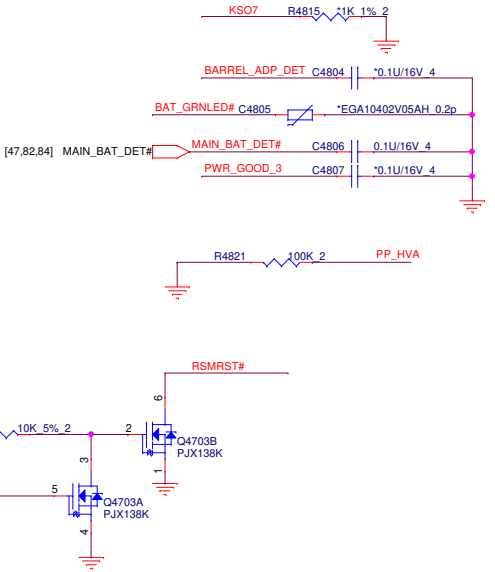


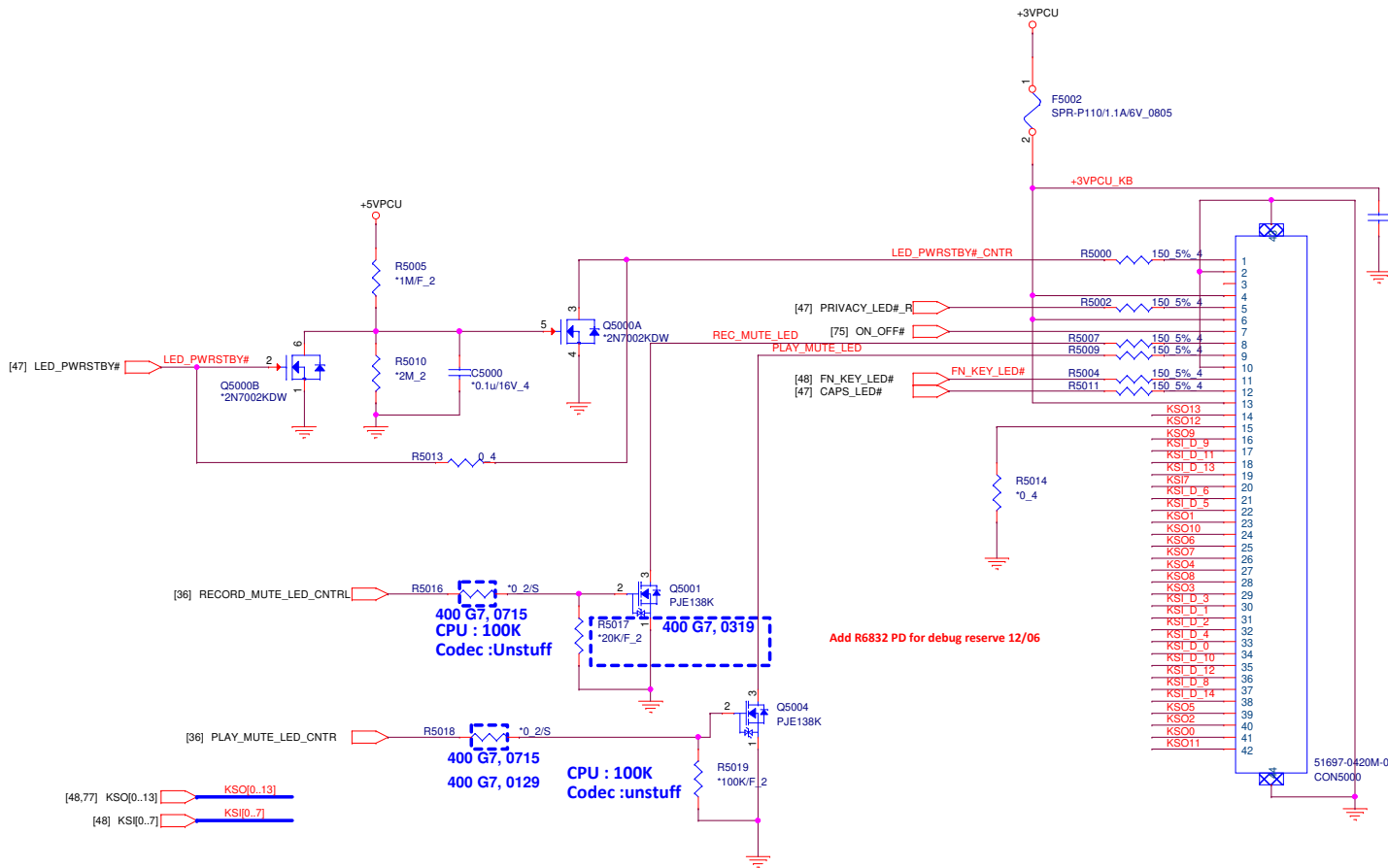
NOTE : IF INSTALL R10603, PLEASE UNINSTALL R224

R4824 (Kohm, 1%)	"PLT_DET" CONFIGURATION SETTING
137 (CS41371FE01)	CS U22 UMA SKU
80.6 (CS38061FE00)	CS U22 DIS SKU
51.1 (CS35111FE05)	CS U42/U62 UMA SKU
34 (CS33401FE01)	CS U42/U62 DIS SKU

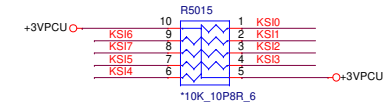


ESD SOLUTION

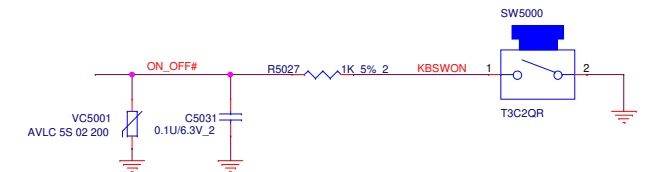
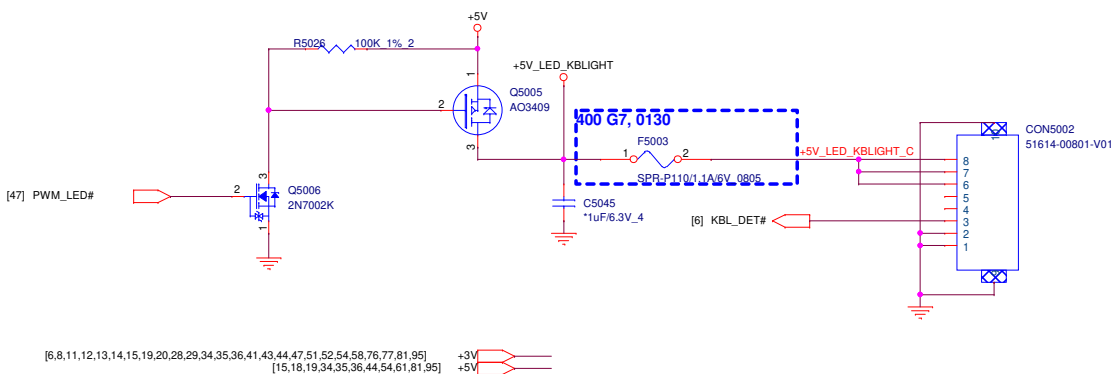




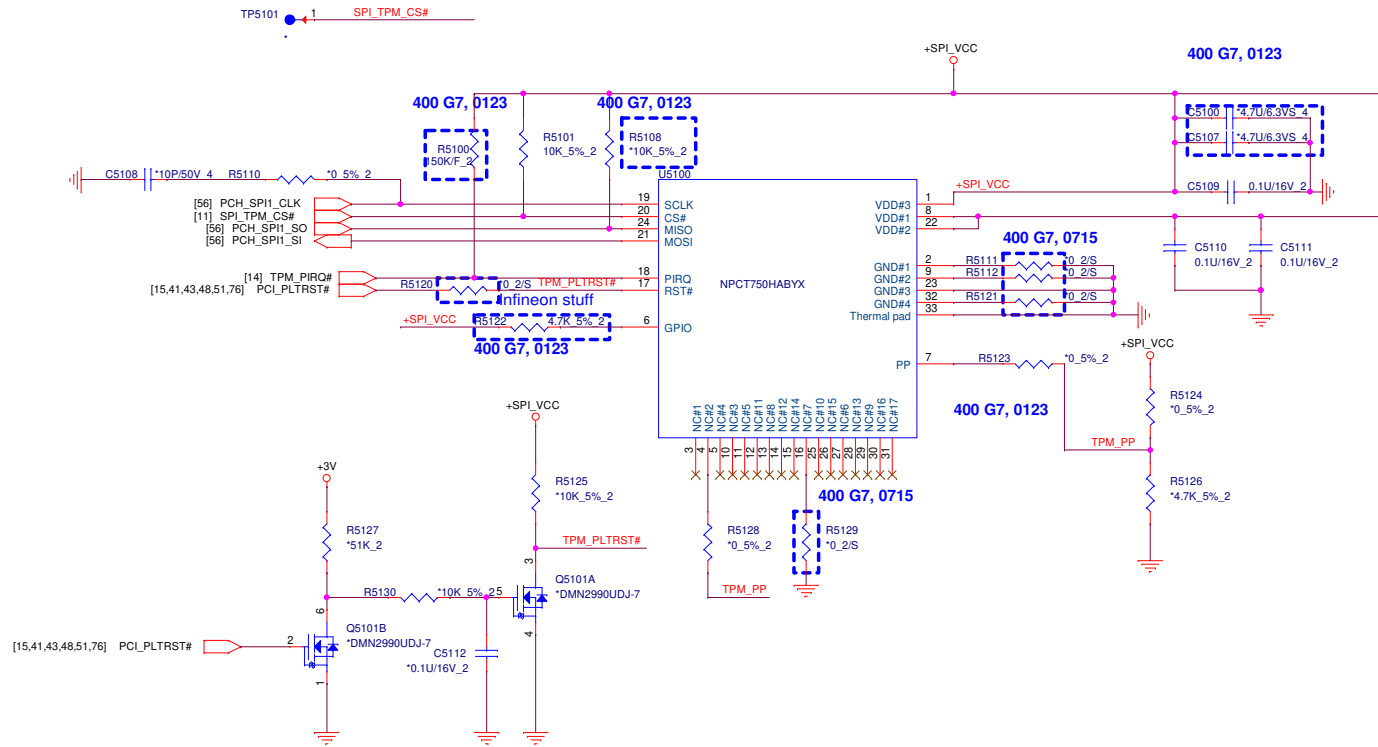
KEYBOARD PULL-UP



Stuff PW button for test in factory.



TPM (1.2 or 2.0)



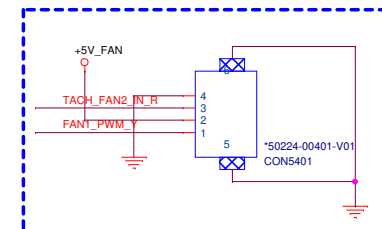
AL000750004
AL000750008--MV AL009670042

	Nuvoton	Infineon
C5106	V	
C5105	V	
R5116	V	
R5113	V	
R5115	V	
R5117		V
R5118		V
R5119		V
R5114		V
R5104		V
R5100	10K	150K



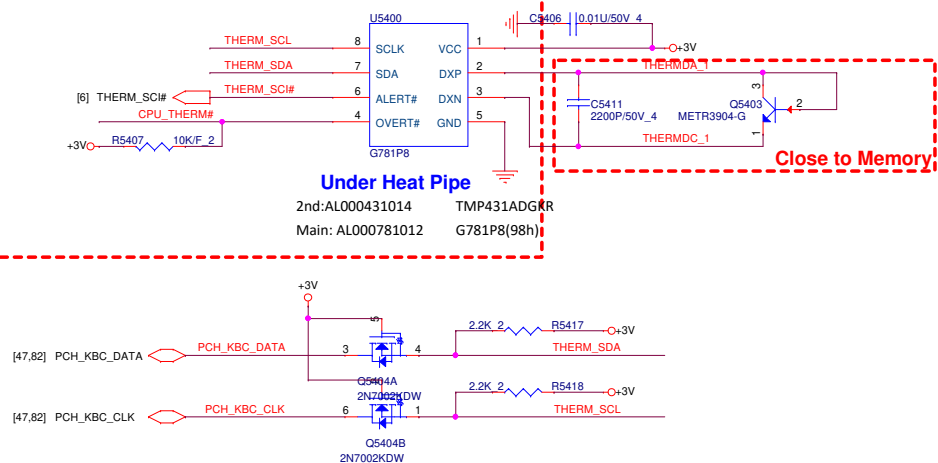
PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 53 -- TS and Accelerometer	Rev 3A
Date: Monday, March 30, 2020		Sheet 53 of 106

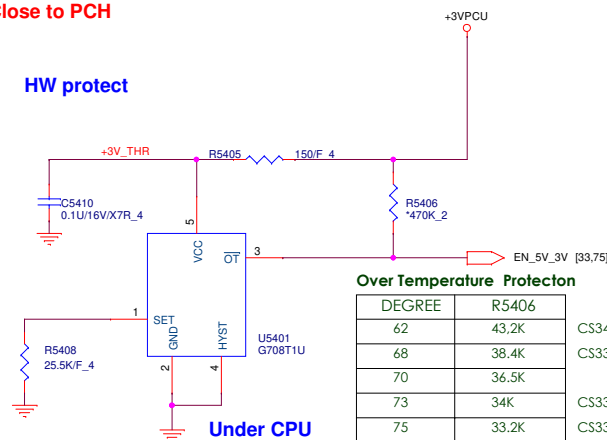


Close to CPU

Under Heat Pipe



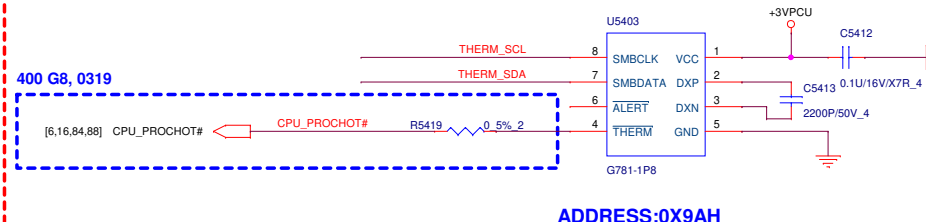
HW protect



Over Temperature Protection			
DEGREE	R5406		
62	43.2K	CS34322FB00	X8I UMA
68	38.4K	CS33832FB08	X8J UMA
70	36.5K		
73	34K	CS33402FB18	X8J N16
75	33.2K	CS33322FB13	
81	28K		
85	25.5K	CS32552FB11	X8J N17

$$R_{SET} \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$

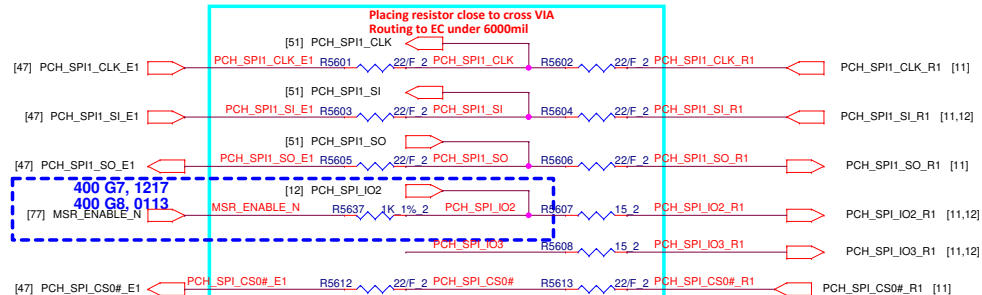
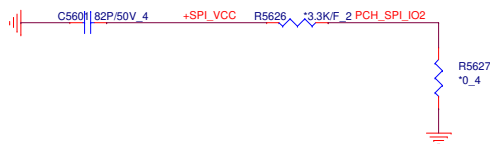
SKIN Thermal Sensor



400 G8, 0319

SPI ROM

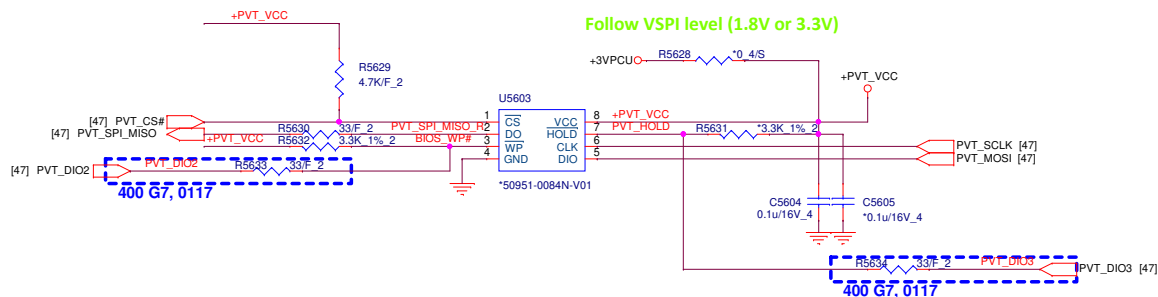
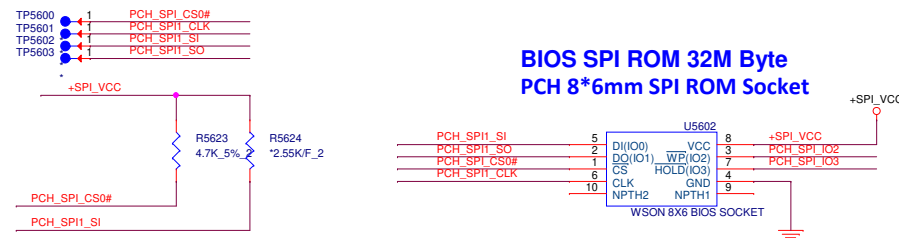
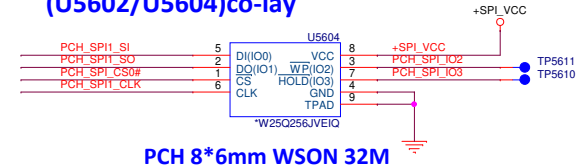
Vender	Size	P/N
MXIC	32MB	AKE3JZ-KZ01
Winbond	32MB	AKE3JF00N00
Socket		DFHS08FS060

PCH SPI ROM(CLG)
Place TP at TOP side

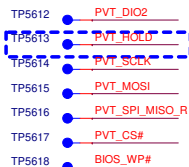
400 G8, 0305

EC SPI ROM Socket WSON 16M 6x5

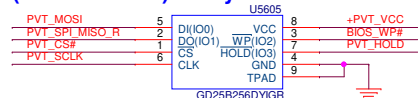
Follow VSPi level (1.8V or 3.3V)

**BIOS SPI ROM 32M Byte**
PCH 8*6mm SPI ROM Socket**SPI ROM 32M 8x6 IC & 8*6 Socket**
(U5602/U5604)co-lay**PCH 8*6mm WSON 32M**

400 G8, 0319



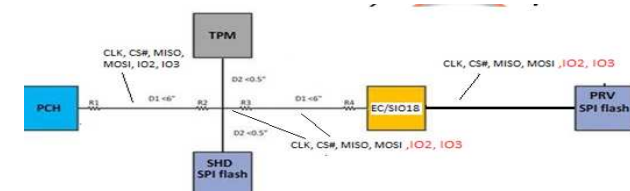
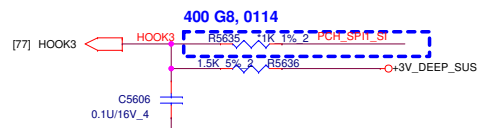
400 G8, 0304

Reserve EC SPI ROM 32M Byte
(U5603/U5605)co-lay

400 G8, 0319

EC SPI ROM

Vender	Size	P/N
GGD	32MB	AKE3JZ00Q02

MV/MP stuff

nuvoton

Nuvoton Confidential - Provided under NDA

Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = Quad I/O, Quad I/O.
R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3
R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3
R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm
R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm

Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.

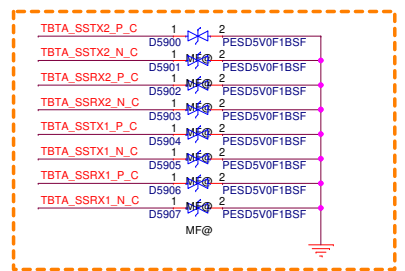


PROJECT : 400_600_G8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	56 - Flash(KBC+PCH)	3A
Date: Tuesday, March 31, 2020	Sheet 56 of 106	

MF Sku Co-lay

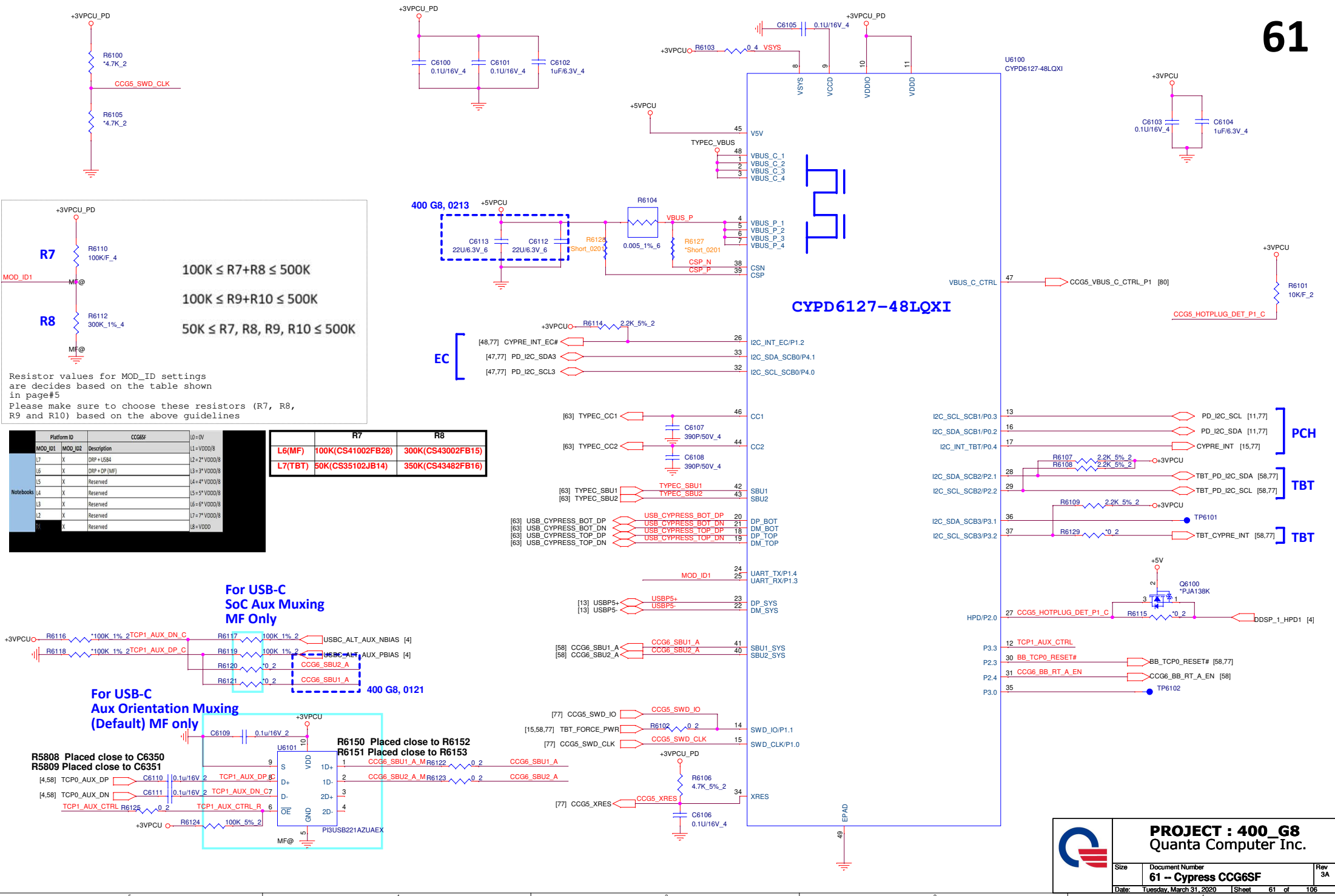
TCP0_TX_P0	R5947	MF@	0	5%	2	TCP0_DIRECT_TX0_R_DP	R5949	MF@	0	5%	2	TBTA_SSTX1_P_C
TCP0_TX_N0	R5950	MF@	0	5%	2	TCP0_DIRECT_TX0_R_DN	R5951	MF@	0	5%	2	TBTA_SSTX1_N_C
TCP0_TXRX_P0	R5952	MF@	0	5%	2	TCP0_DIRECT_TXRX0_R_DP	R5953	MF@	0	5%	2	TBTA_SSRX1_P_C
TCP0_TXRX_N0	R5954	MF@	0	5%	2	TCP0_DIRECT_TXRX0_R_DN	R5955	MF@	0	5%	2	TBTA_SSRX1_N_C
TCP0_TX_P1	R5956	MF@	0	5%	2	TCP0_DIRECT_TX1_R_DP	R5957	MF@	0	5%	2	TBTA_SSTX2_P_C
TCP0_TX_N1	R5958	MF@	0	5%	2	TCP0_DIRECT_TX1_R_DN	R5959	MF@	0	5%	2	TBTA_SSTX2_N_C
TCP0_TXRX_P1	R5960	MF@	0	5%	2	TCP0_DIRECT_TXRX1_R_DP	R5961	MF@	0	5%	2	TBTA_SSRX2_P_C
TCP0_TXRX_N1	R5962	MF@	0	5%	2	TCP0_DIRECT_TXRX1_R_DN	R5963	MF@	0	5%	2	TBTA_SSRX2_N_C





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Quanta Computer Inc.

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USB Charging Port

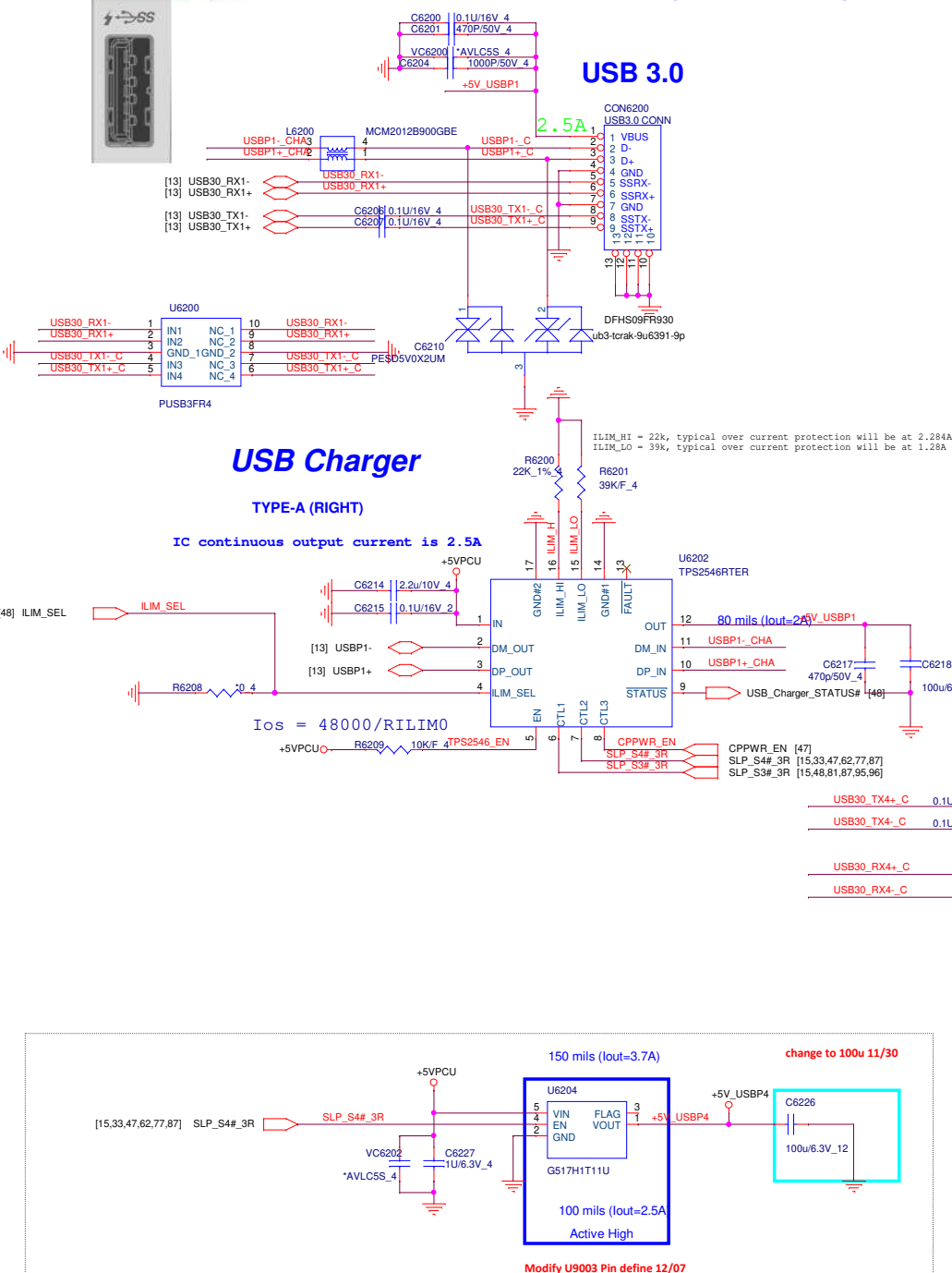
USB 2.0/3.0 Combo

Right for charge

USB Power Port

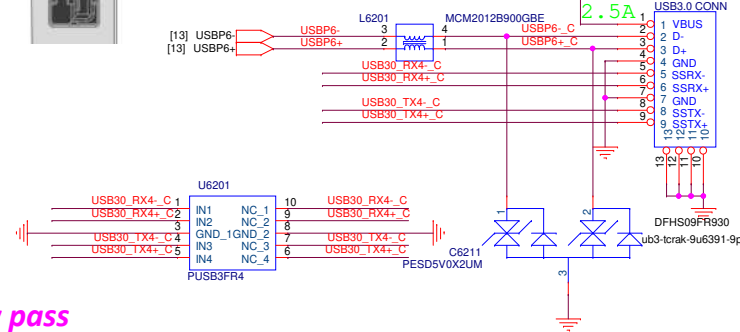
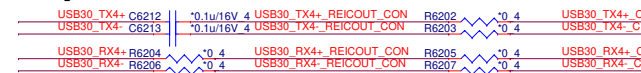
USB 2.0/3.0 Combo

Left



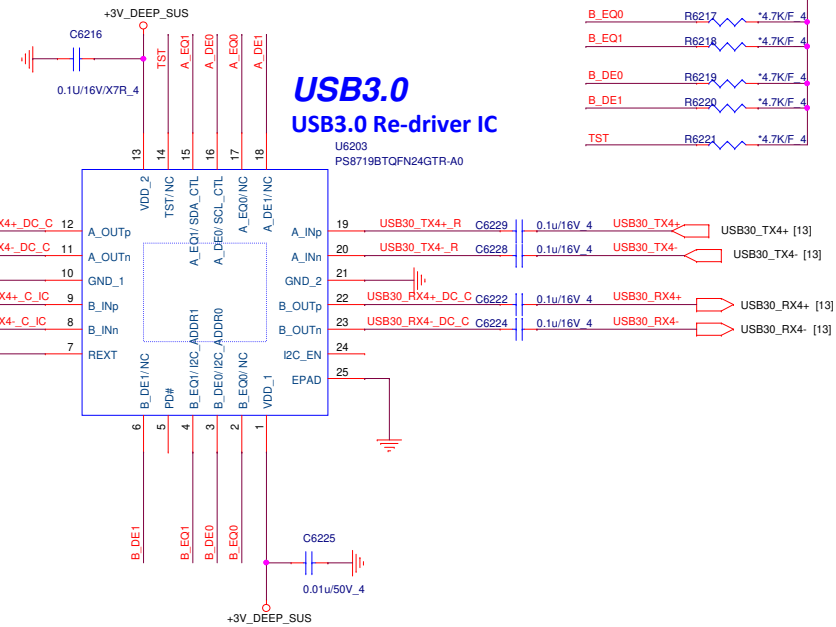
13" By pass

Co-layout



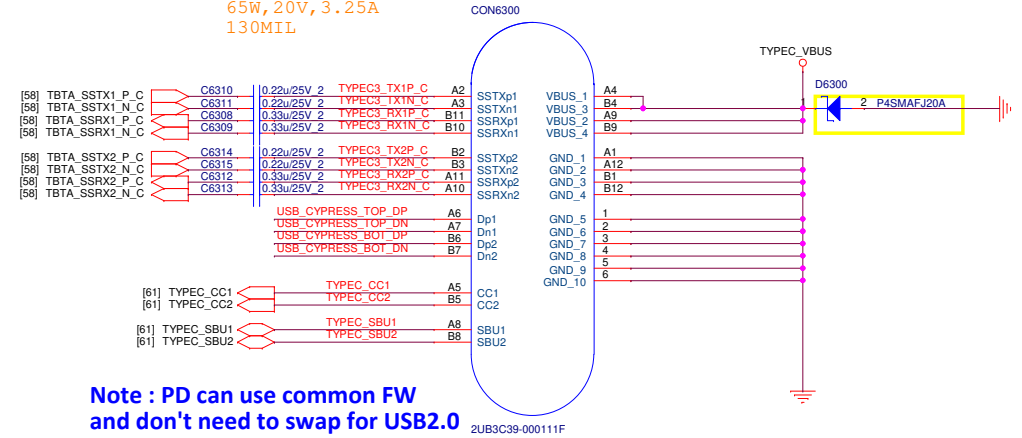
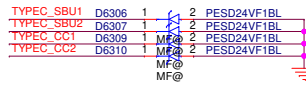
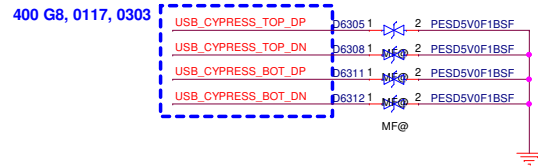
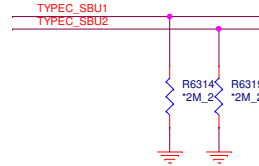
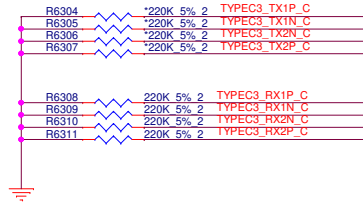
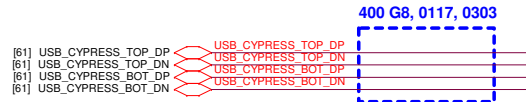
USB3.0

USB3.0 Re-driver IC



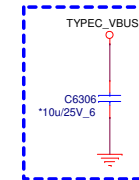
			PROJECT : 400_G8 Quanta Computer Inc.	
Size	Document Number	Rev		3A
Date:	Monday, March 30, 2020	Sheet	62 of	106

USB Type-C Port A

65W, 20V, 3.25A
130MIL

Note : PD can use common FW
and don't need to swap for USB2.0

400 G8, 0213





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Quanta Computer Inc.

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Quanta Computer Inc.

Size Custom	Document Number N17S-G1-A1(MEMORY/GND)	Rev
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	PROJECT : 400_G8 Quanta Computer Inc.		
	Size Custom	Document Number N17S-G1-A1(DISPLAY)	Rev
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Quanta Computer Inc.

Size Custom	Document Number N17S-G1-A1(GPIO/STRAPS)	Rev
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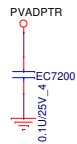
PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 23 -- VRAM GDDR5 - RANK1	Rev 1A
Date: Monday, March 30, 2020		Sheet 70 of 106



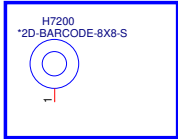
PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 24 -- VRAM CONFIG	Rev 1A
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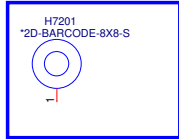


13" Hole Shielding CAP

2DBarcode

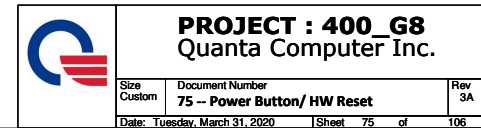


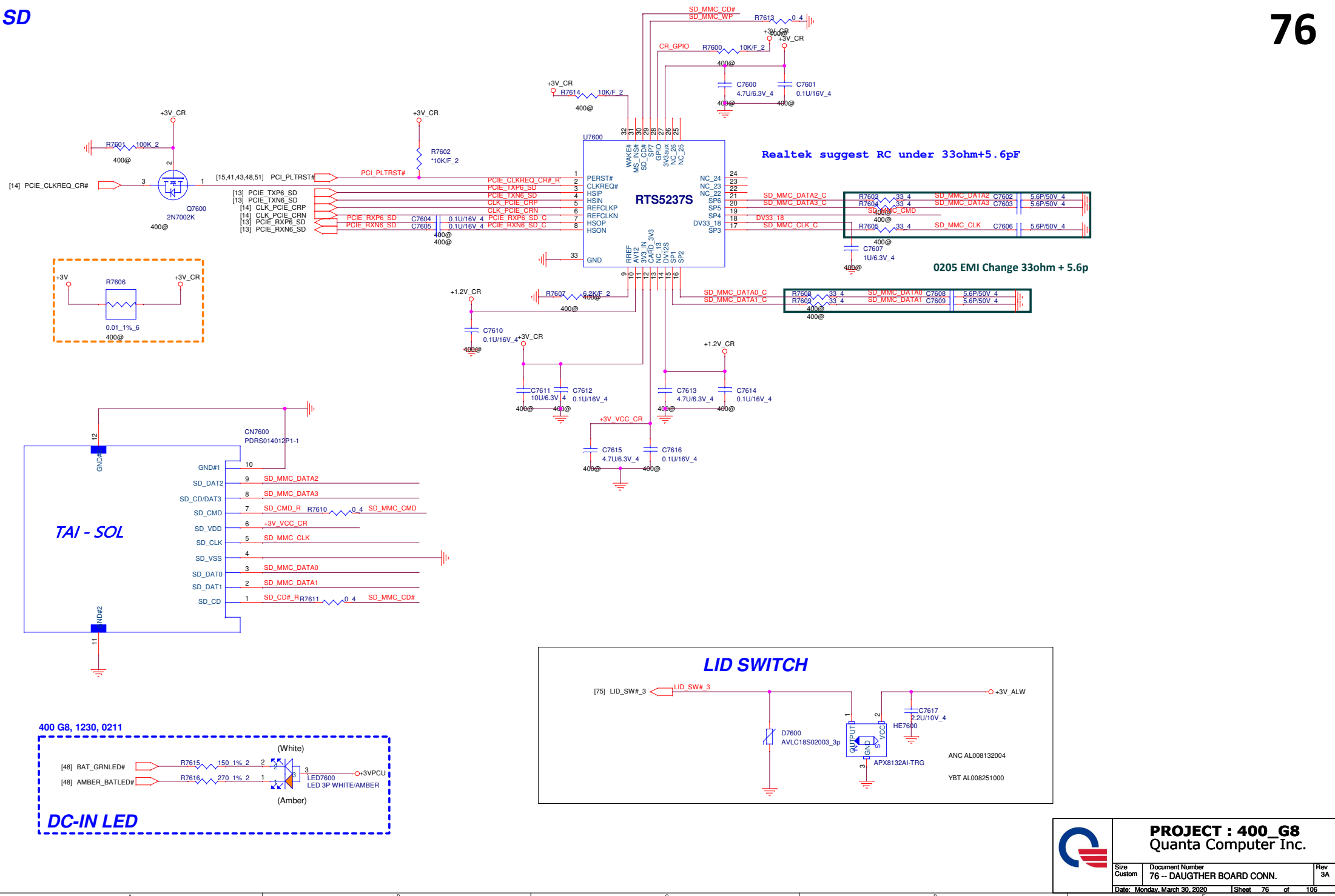
2DBarcode



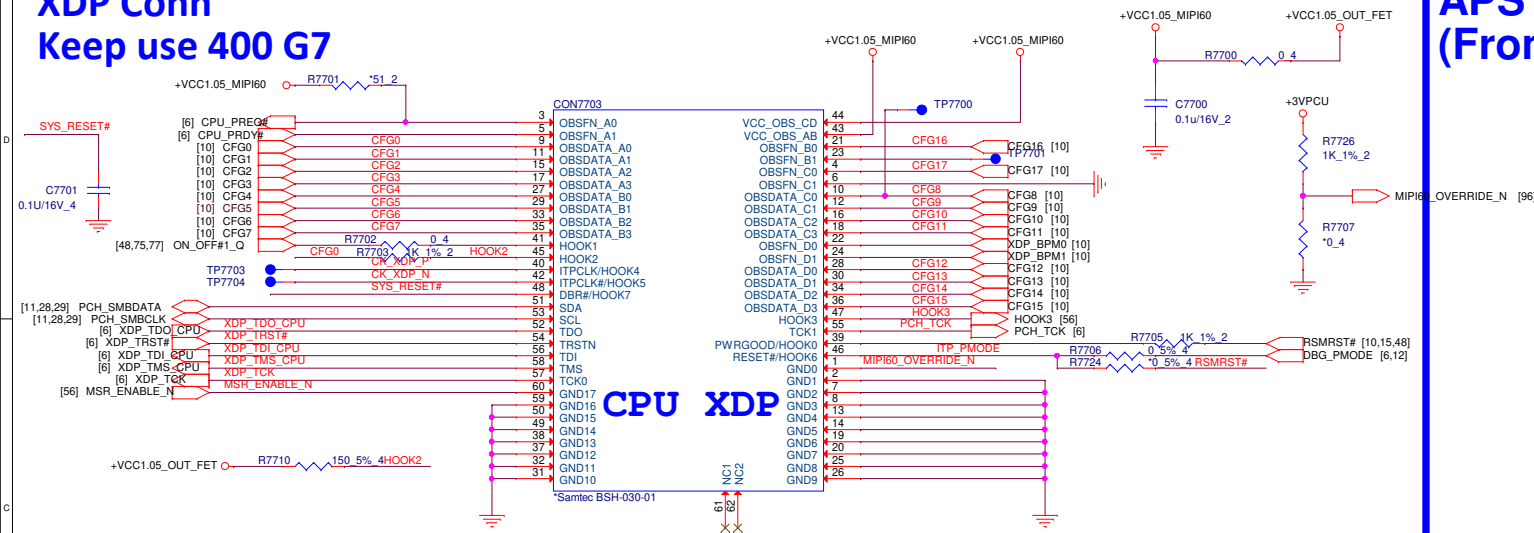
PROJECT : 400_G8
Quanta Computer Inc.

Size Custom	Document Number 72 – EMI/RF CAP (13 UMA)	Rev 3A
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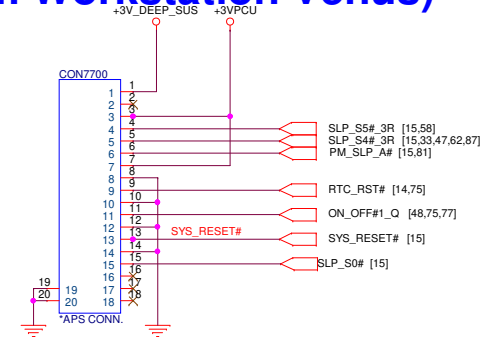


XDP Conn
Keep use 400 G7

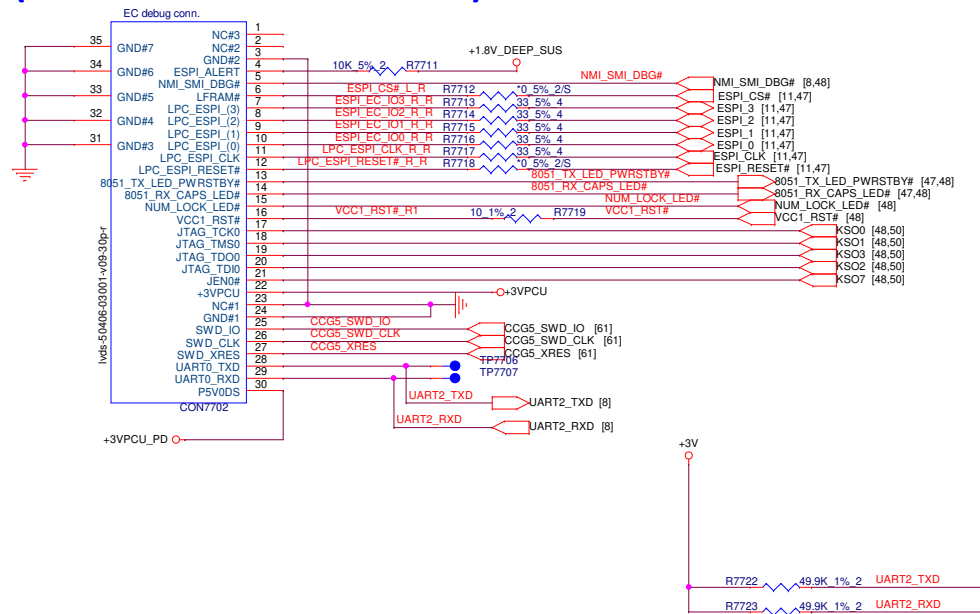


APS (From Workstation Venus)

77

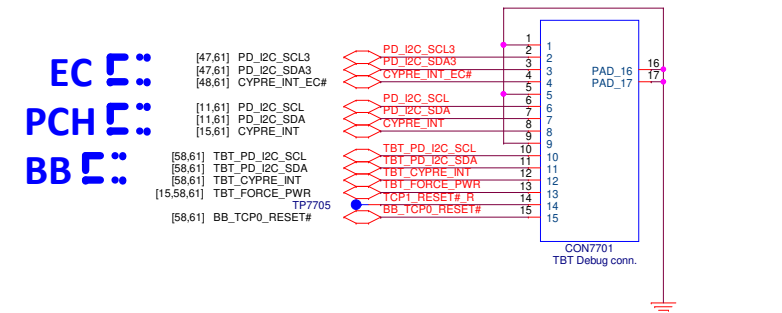


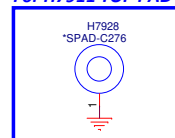
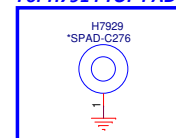
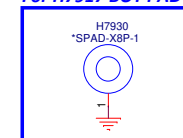
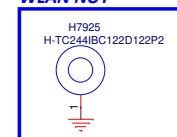
EC debug conn. (From Workstation Venus)

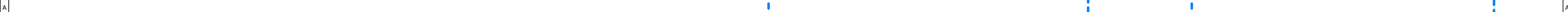


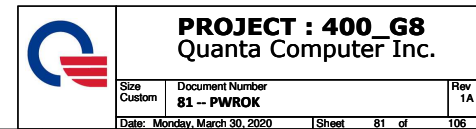
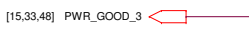
TYPE-C Debug connector

TBT Debug conn.

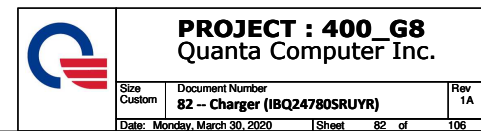


Hole**For H7911 TOP PAD****For H7914 TOP PAD****For H7917 BOT PAD****WLAN NUT****SSD NUT**





82

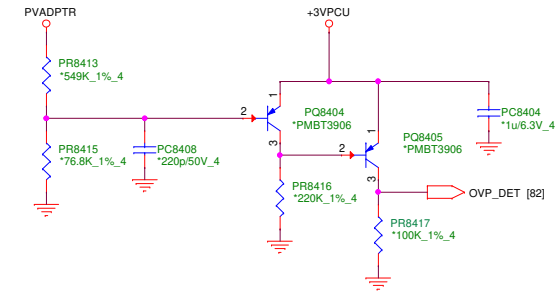
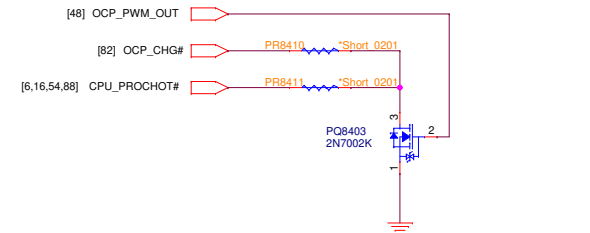
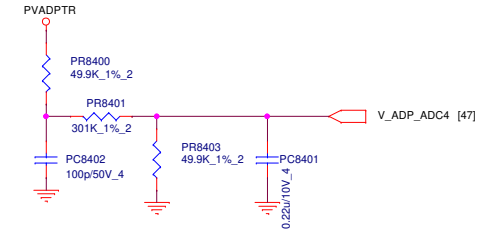
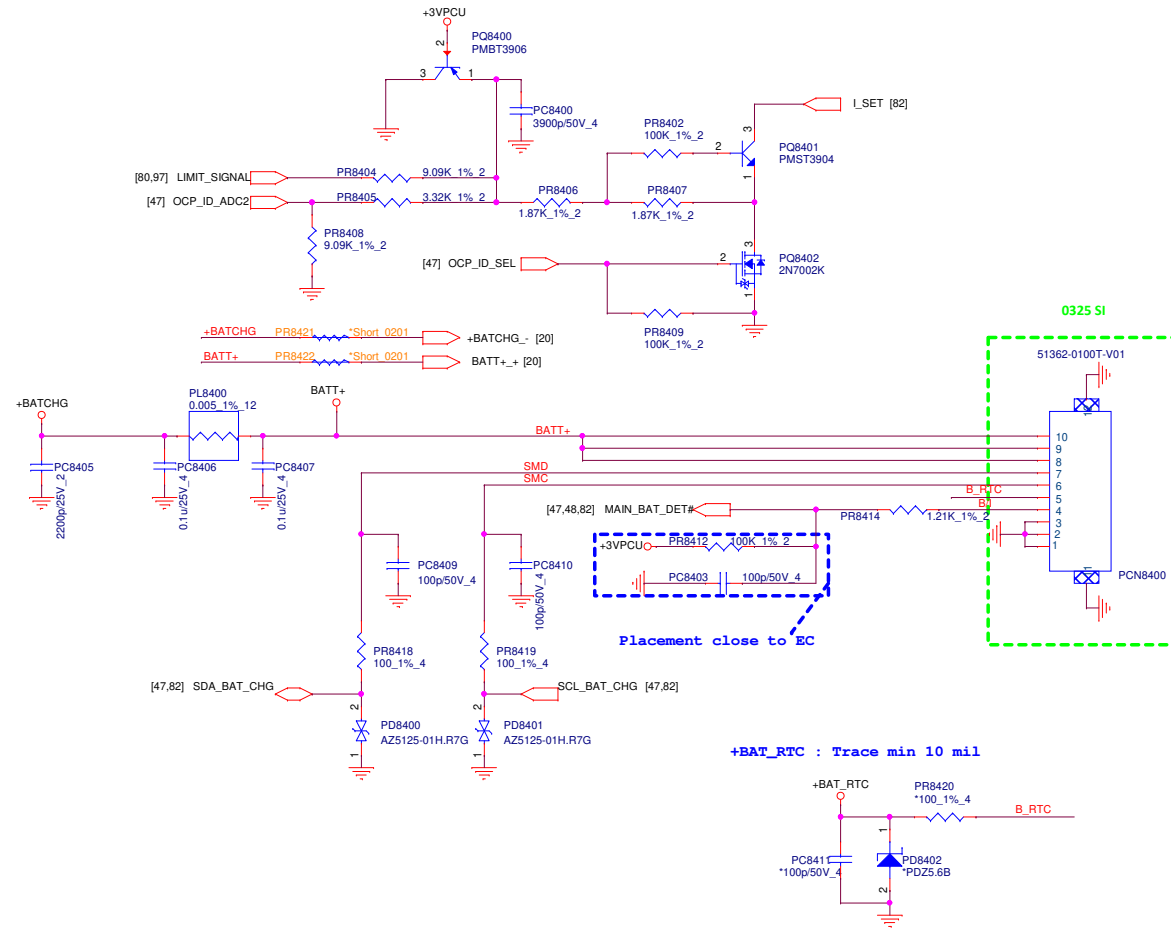




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Quanta Computer Inc.

Size Custom	Document Number 83 -- Charger (ISL9538HRTZ-T)	Rev 1A
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Barrel Adapter OCP

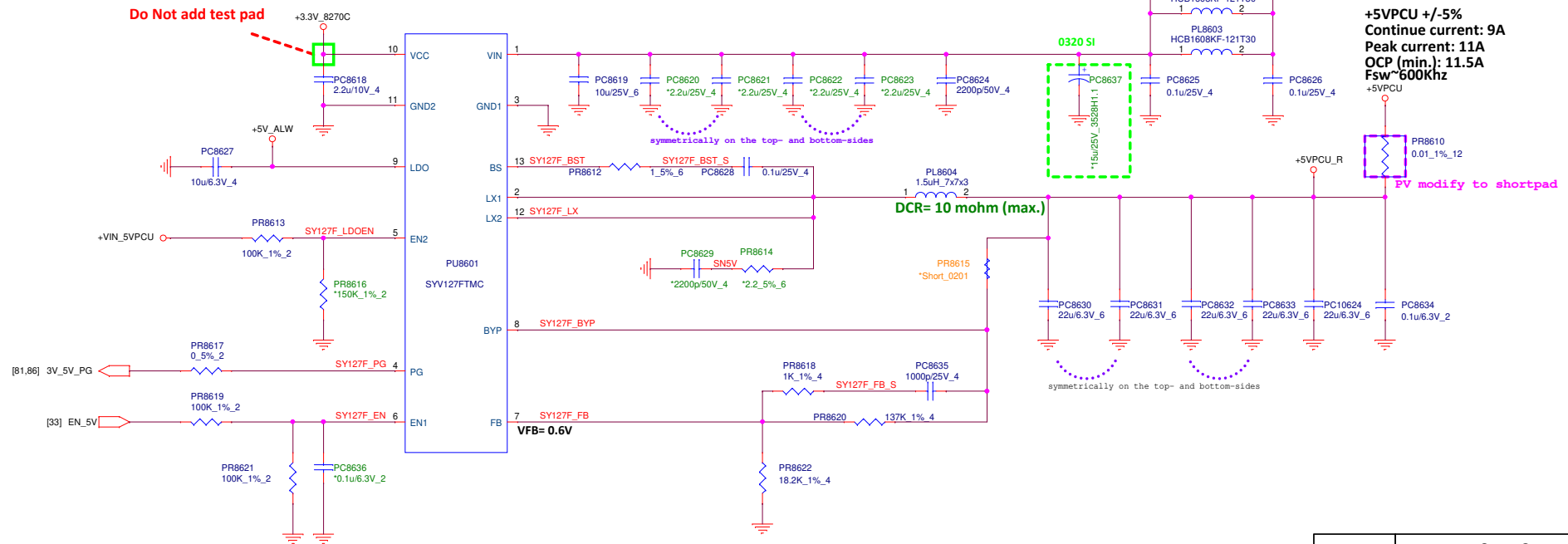
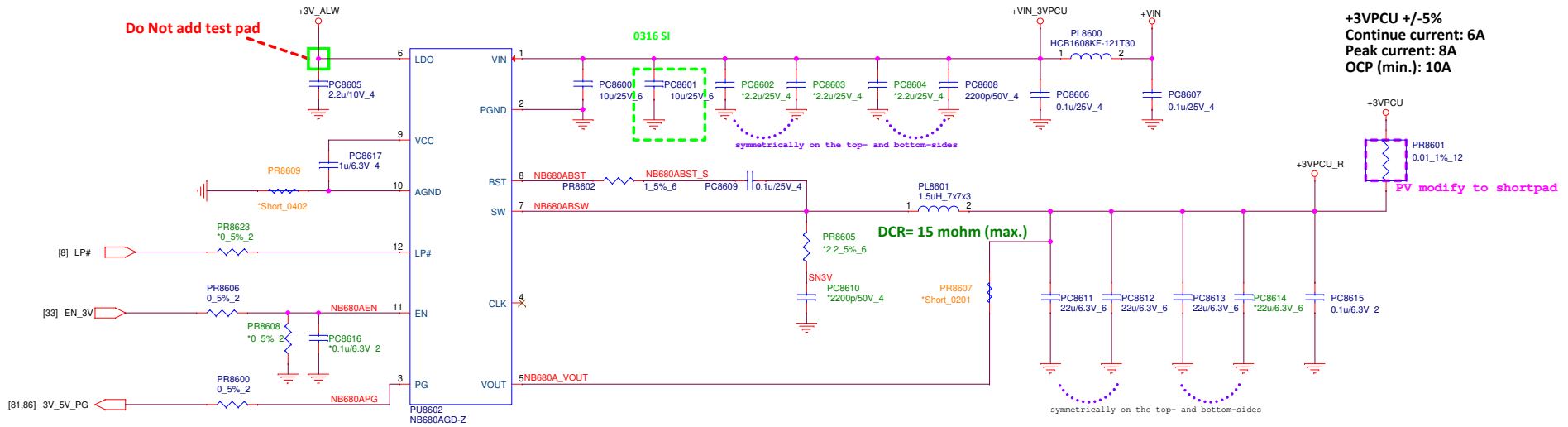




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Quanta Computer Inc.

Size Custom	Document Number 85 -- Charger II	Rev 1A
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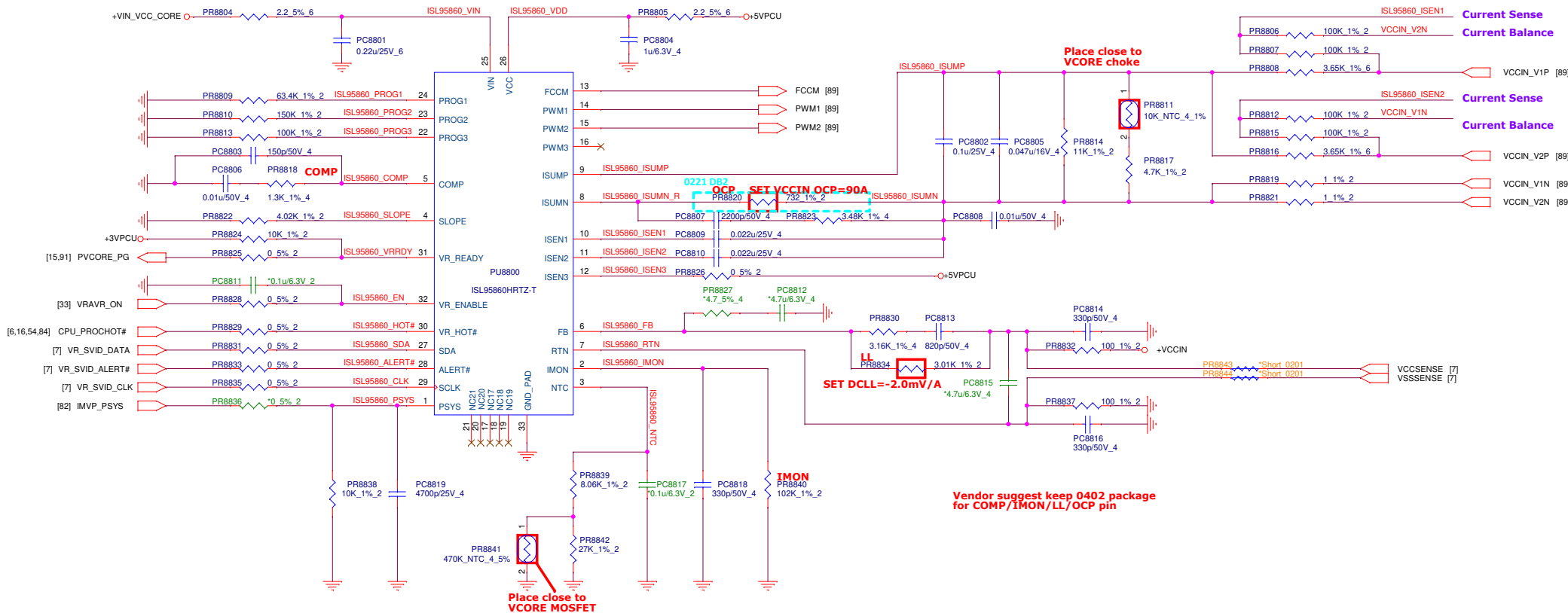


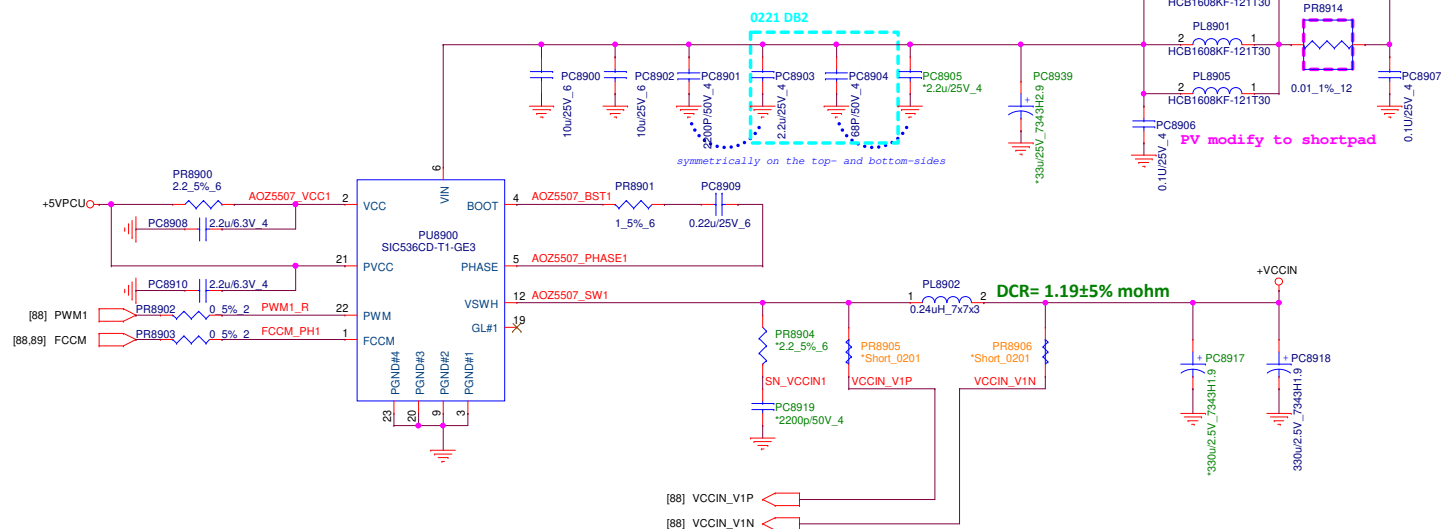
[8,10,15,16,18,19,33,34,36,41,44,47,48,50,52,54,56,58,61,75,76,77,80,81,82,84,87,88,91,92,95,96] +3VPCU
 [18,48,50,61,62,81,87,88,89,91,95,96] +5VPCU
 [34,81,82,87,92,97,106] +VIN



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	86 -- +3/5VSS(SY8286B/SY8286C)	1A
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IMVP9 Design: TGL UP3 4+2 (15W)_Performance line
2-phase, Inductor DCR Sensing

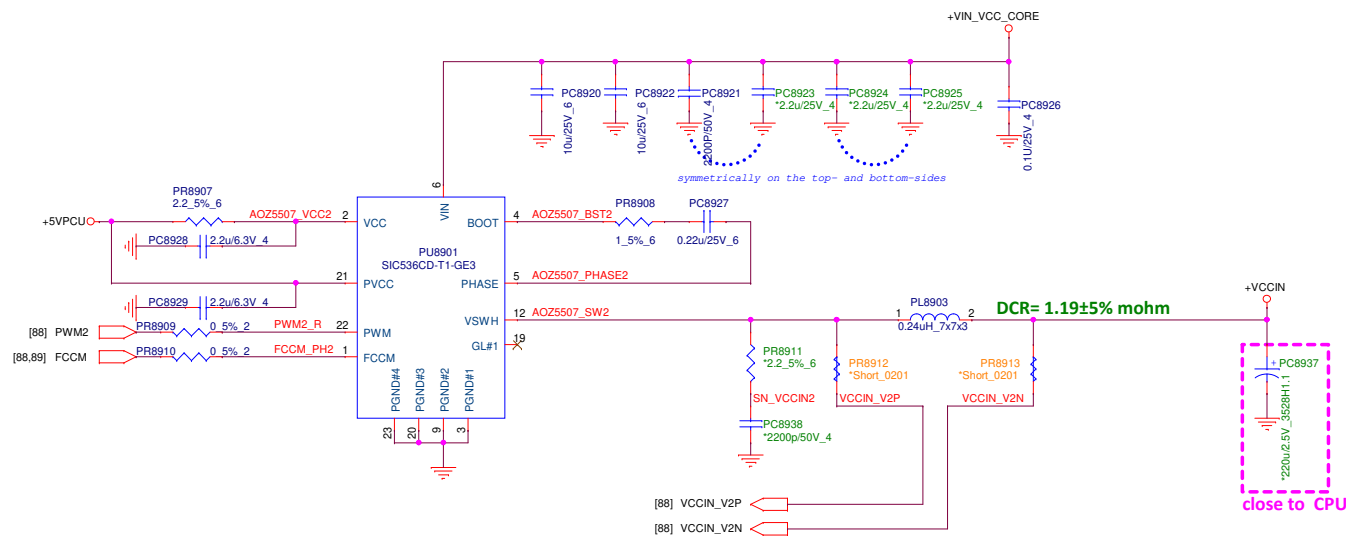
Ref DOC#: 607872 & 575683

VCCIN rail
TDC=36A
Iccmax=55A
Iccmax Transient=65A (10mS)
OCP(min)=90A
DCLL= 2.0mohm
ACLL= 4.4mohm

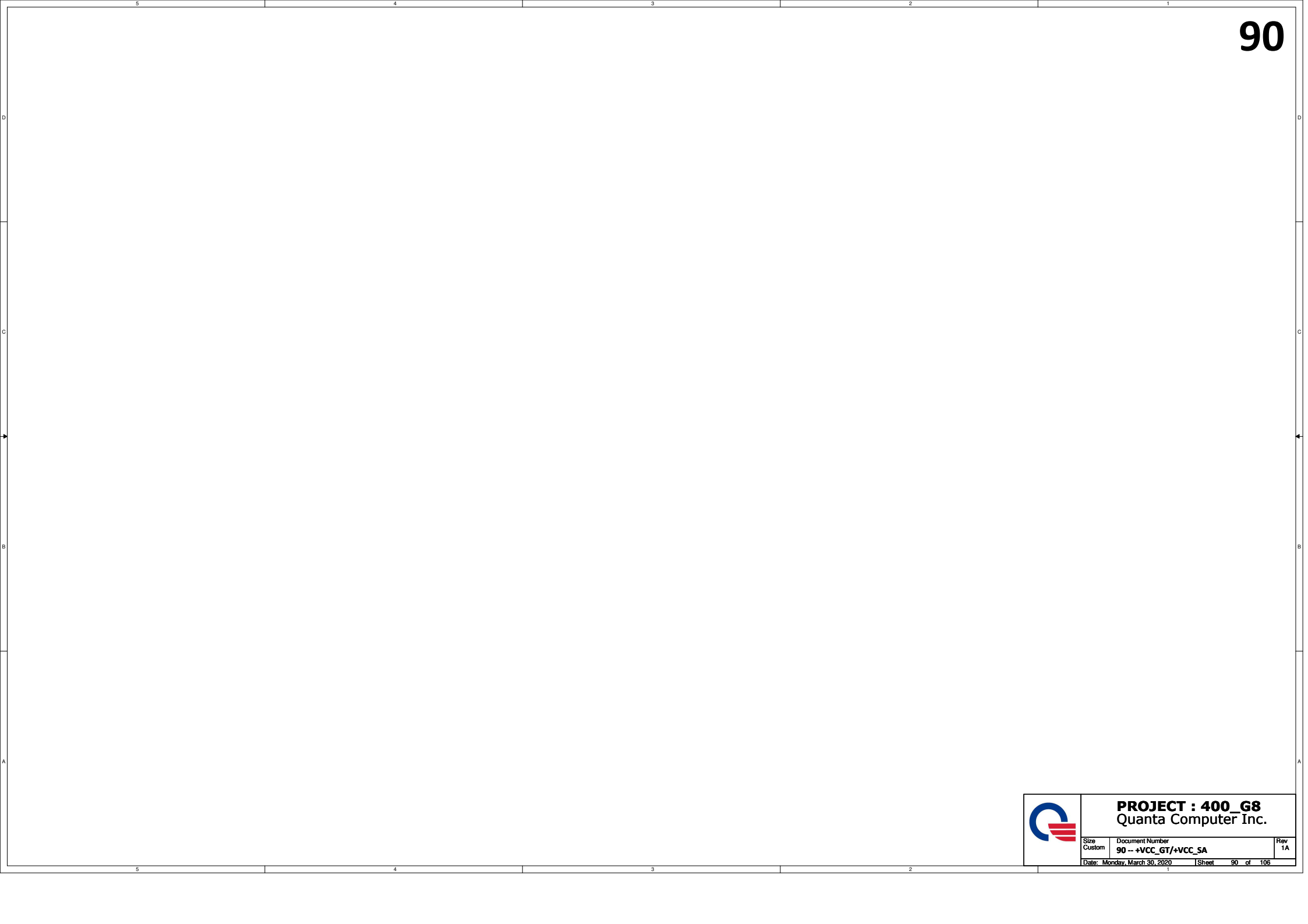
Renesas recommended quantity
22u/6.3V_6 x10pcs
330u/2V_7343H1.9 x1pcs
Total 550u

CPU side install
22u/6.3V_6 x9pcs
10u/6.3V_6 x25pcs
Total 448u
Power side install
330u/2V_7343H1.9 x1pcs
Total 330u
EE+Power = 748u

Total install can meet Renesas require



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	Quanta Computer Inc.		
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	Size Custom	Document Number 90 -- +VCC_GT/+VCC_SA
	Date: Monday, March 30, 2020	

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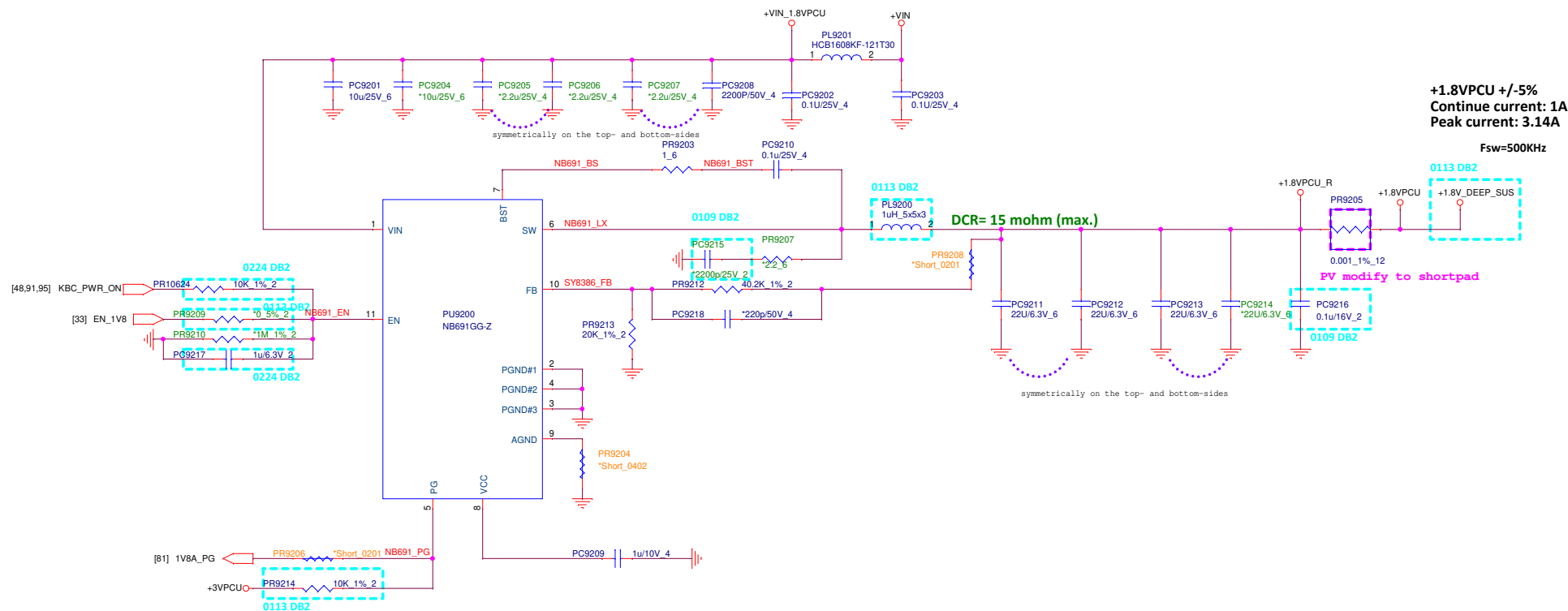


3

Tabel---4:VID control Bit logics

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8



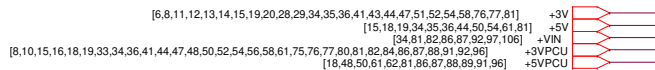
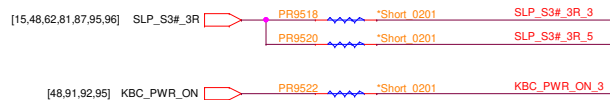
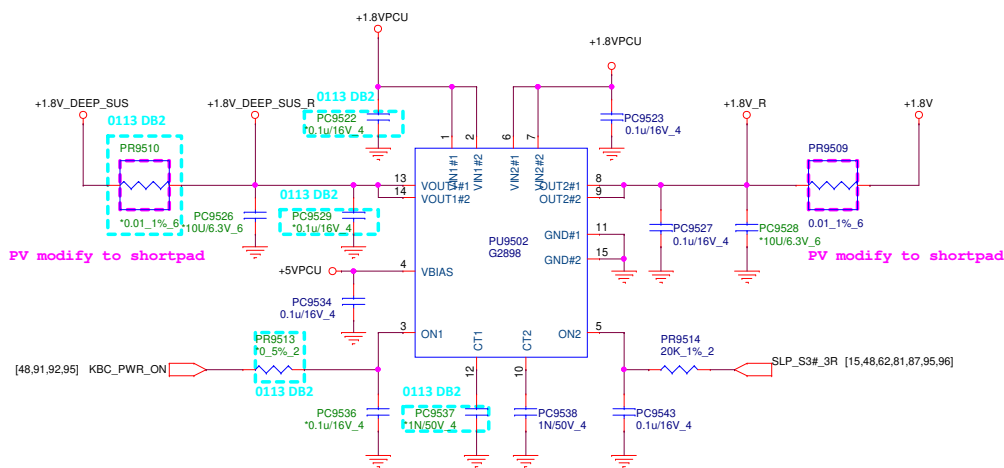
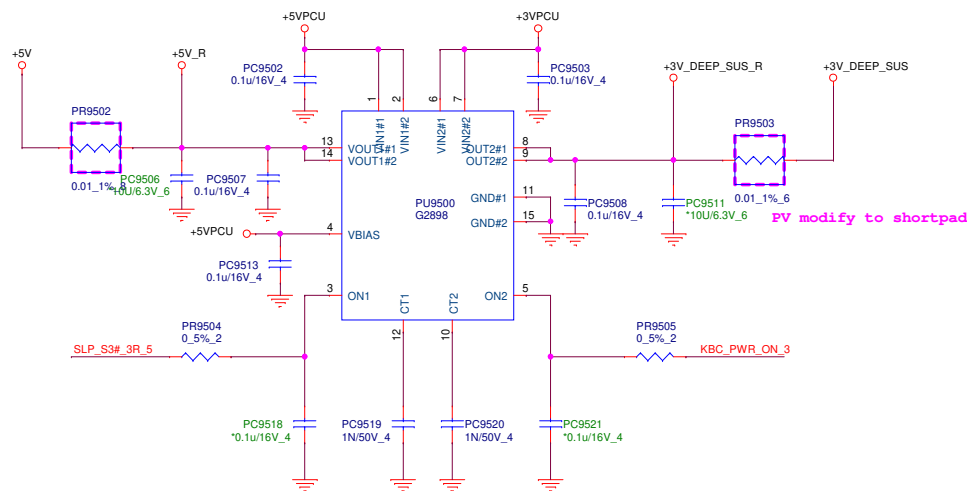
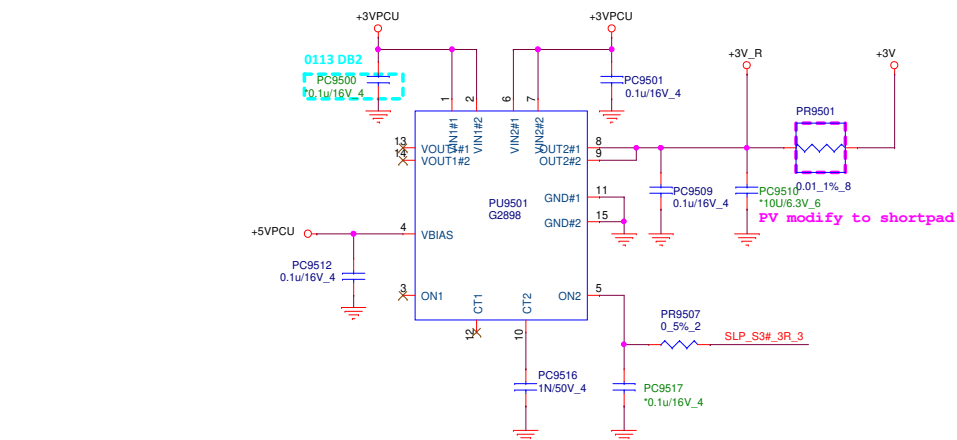
Note: LP#, CO and C1 are pulled high internally

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Size Custom	Document Number 94 -- reserve page	Rev 1A
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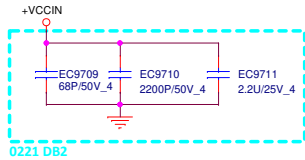
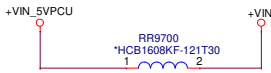
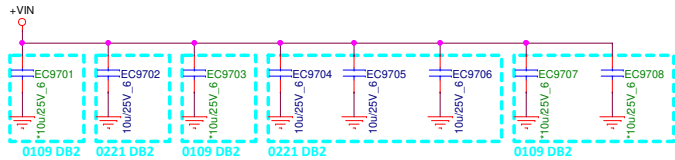
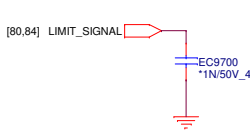


		PROJECT : 400_G8	
		Quanta Computer Inc.	
Size	Document Number	95 - Load Switch I (AOZ1331DI)	Rev 1A
Custom			
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Reserve for EMI & ISEN test

RF Cap



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Quanta Computer Inc.

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Quanta Computer Inc.

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	Size Custom	Document Number A2 -- reserve page	Rev 1A
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	PROJECT : 400_G8 Quanta Computer Inc.		
	Size Custom	Document Number A3 -- reserve page	Rev 1A
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Size Custom	Document Number A5 -- reserve page(N.A)	Rev 1A
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